Highly Compact and Scalable 100 ps CTR + 3D Positioning TOF-PET Detector Sub-Unit

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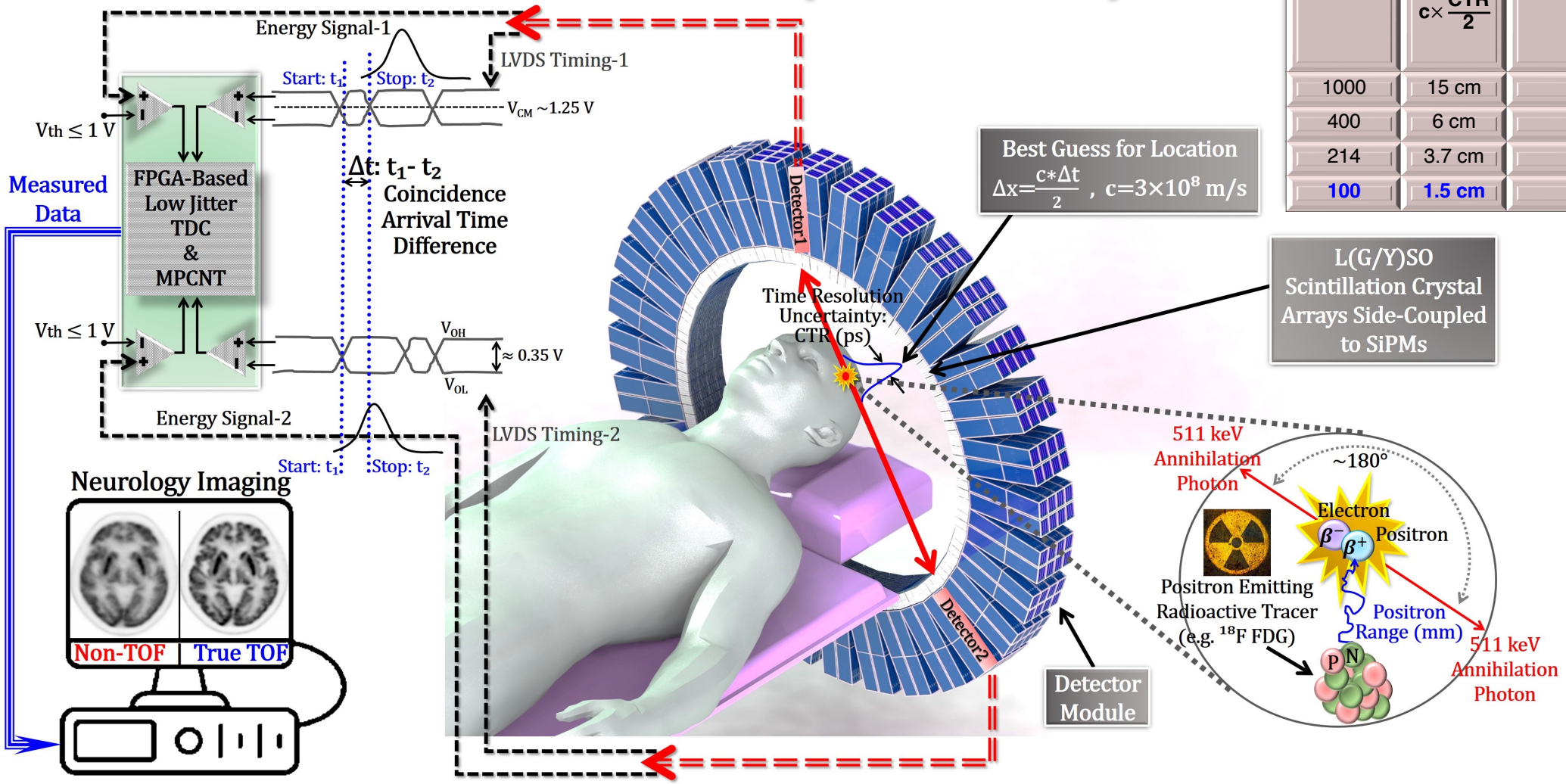
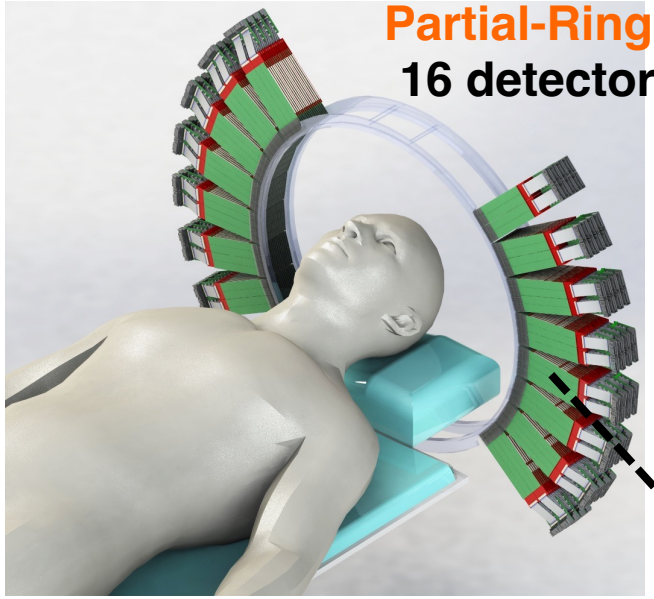
Time of Flight Positron Emission Tomography (TOF-PET)

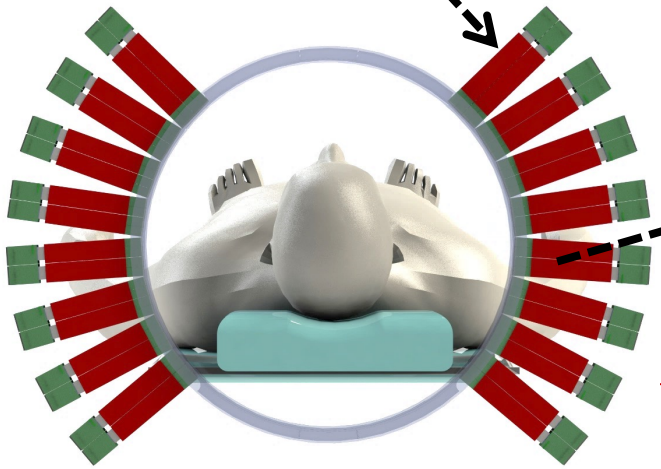
CTR (ps)	$\Delta x = c \times \frac{CTR}{2}$	$Gain = \frac{SNR_{TOF}}{SNR_{Non-TOF}} \approx \sqrt{\frac{D}{c \times \frac{CTR}{2}}}$
1000	15 cm	1.6
400	6 cm	2.6
214	3.7 cm	3.5
100	**1.5 cm**	**5.2**



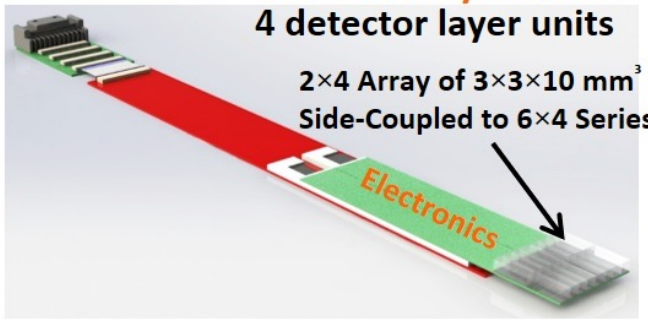
Goal: Scale-Up Side-Readout Modules of 100 ps CTR TOF-PET

- S. Pourashraf, et al, IEEE TRPMS, 2023
- S. Pourashraf, et al, IEEE TRPMS, 2022
- S. Pourashraf, et al, Physics in Medicine and Biology, 2021

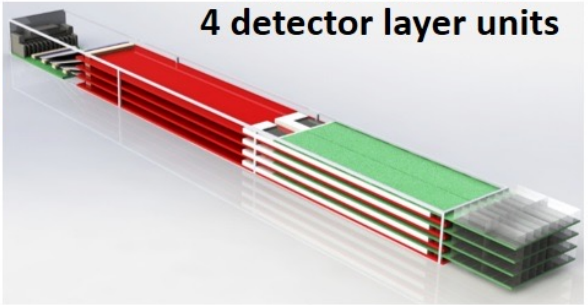




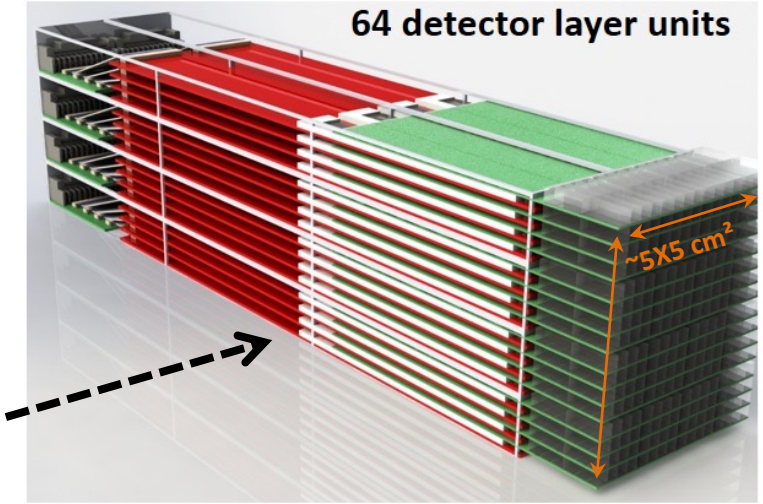
Detector Layer Unit:
4 detector layer units



Sub-Module Unit
4 detector layer units



Detector Module
64 detector layer units



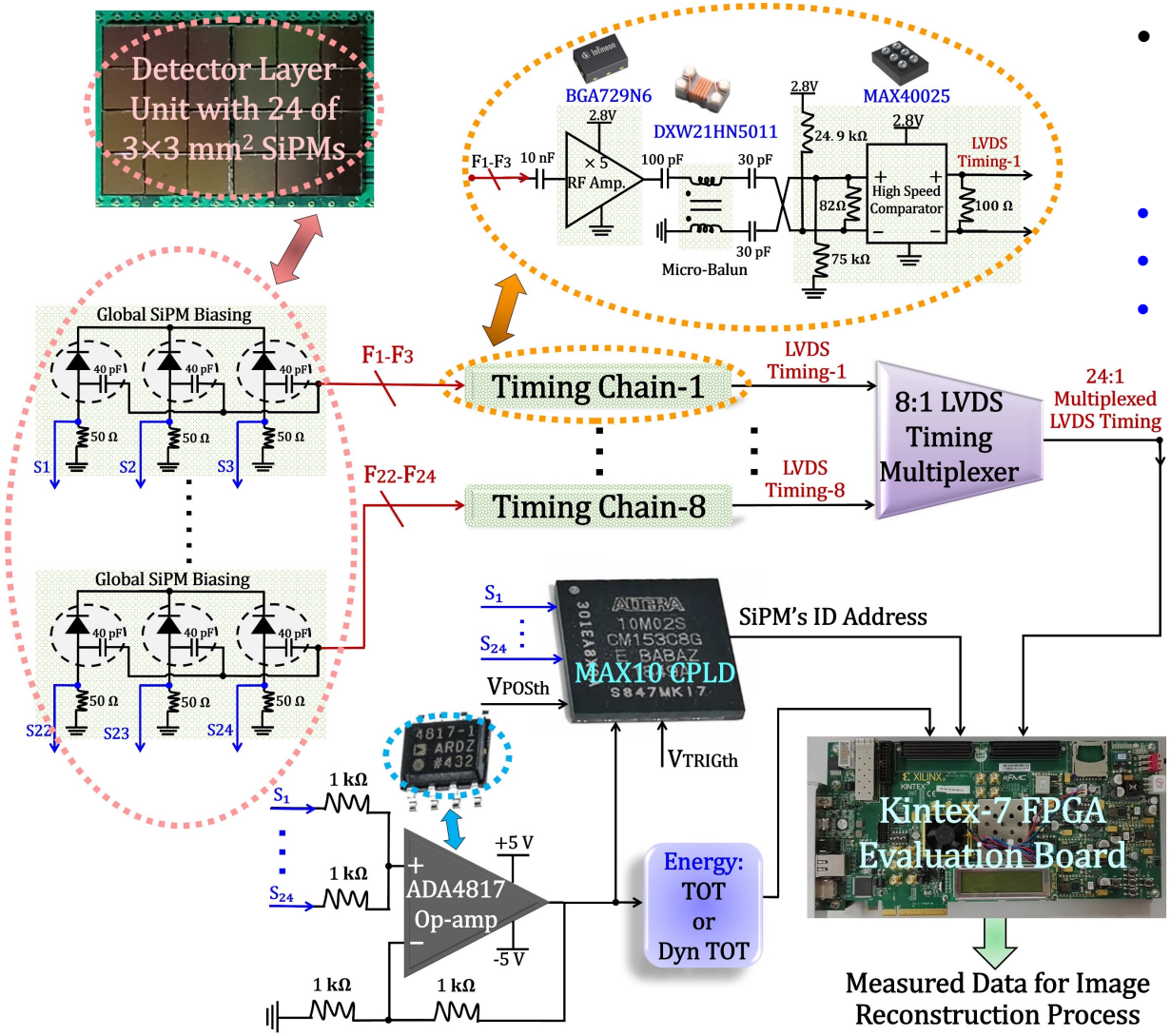
64 Timing

32 Energy

MIPS
Molecular
Program a

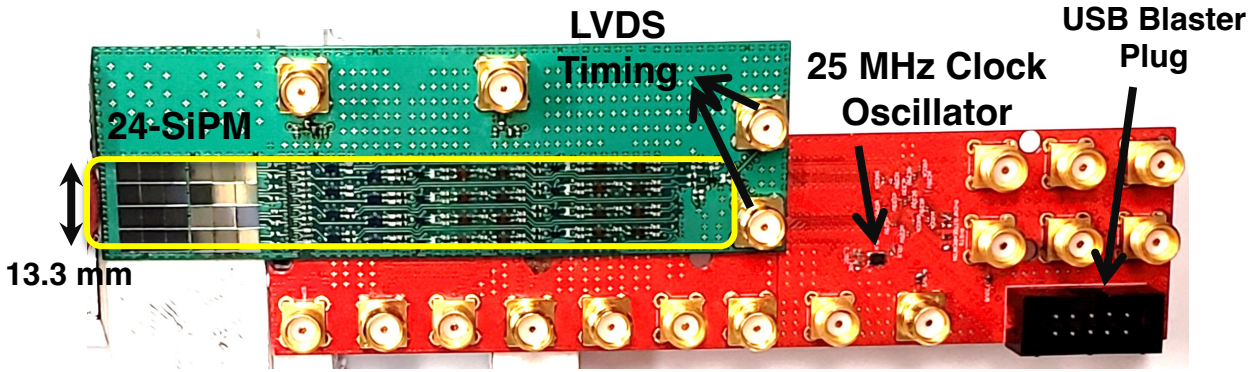
Stanford University
School of Medicine
Department of Radiology

Electronic of Side-Readout Detector Layer Unit

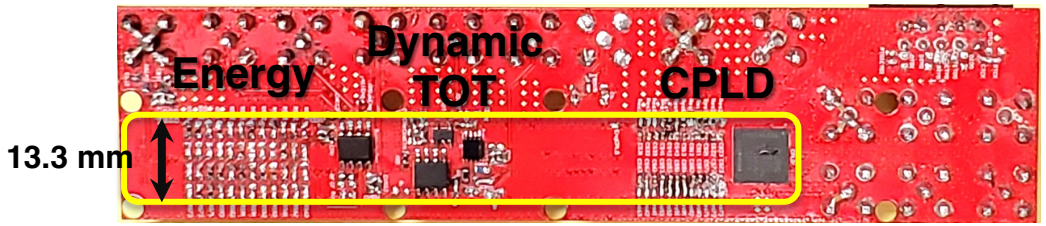


- Hardwired each 3 SiPM fast outputs
  - Creating a 24:8 multiplexing ratio

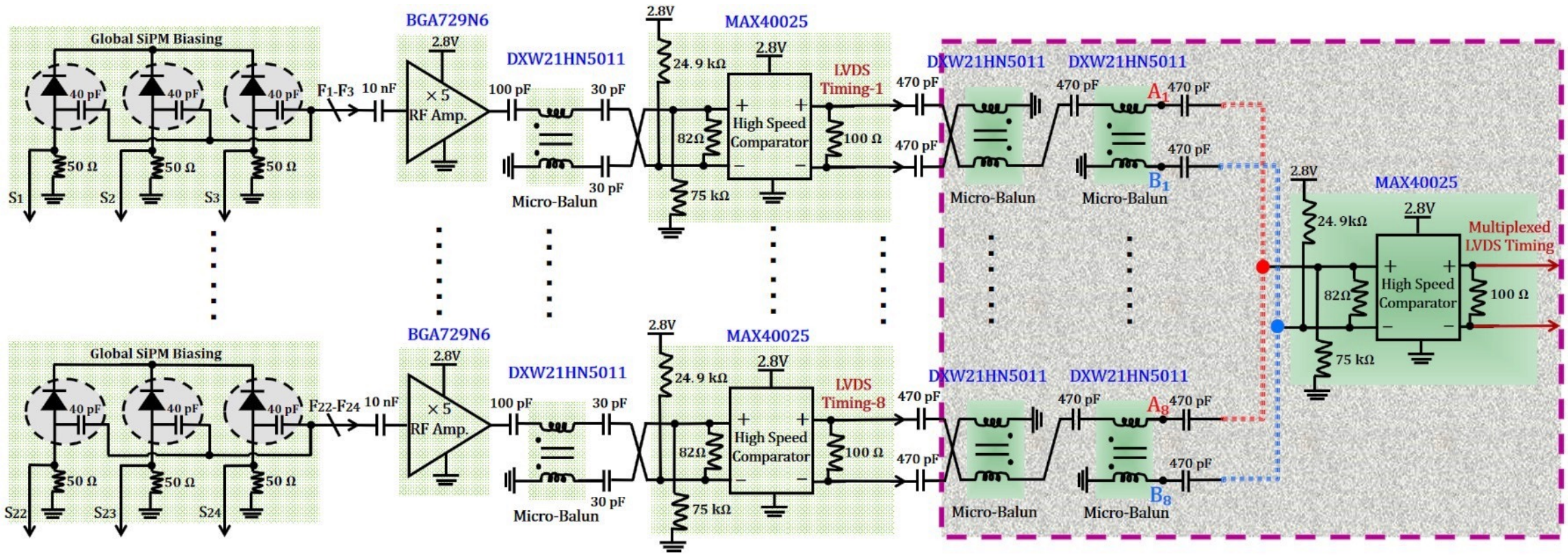
- S. Pourashraf, et al, IEEE TRPMS, 2023
- S. Pourashraf, et al, IEEE TRPMS, 2022
- S. Pourashraf, et al, Physics in Medicine and Biology, 2021



Back of Red Board:



Our 24:1 Timing Multiplexing Approach

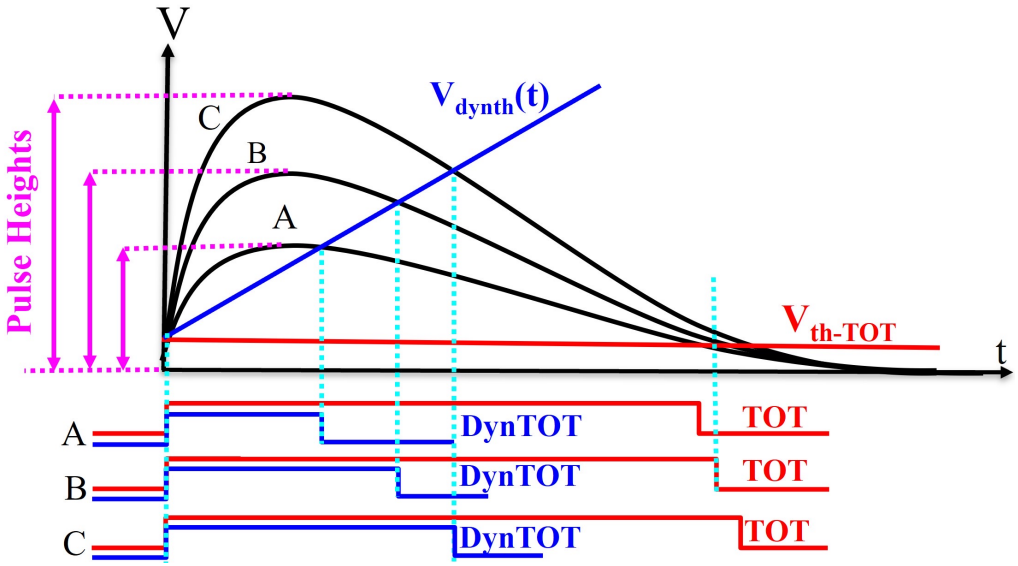


- **Only passive micro-baluns and one extra comparator used**

  -Saving footprint -Cost effective -Power efficient -Kept 100 ps CTR

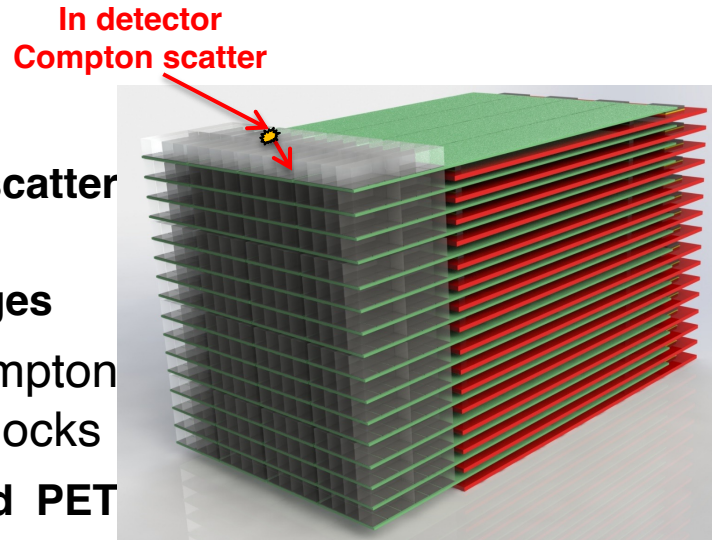
  Just 4.5 mW/Channel extra power dissipation!

Adapted DynTOT Block in our TOF-PET

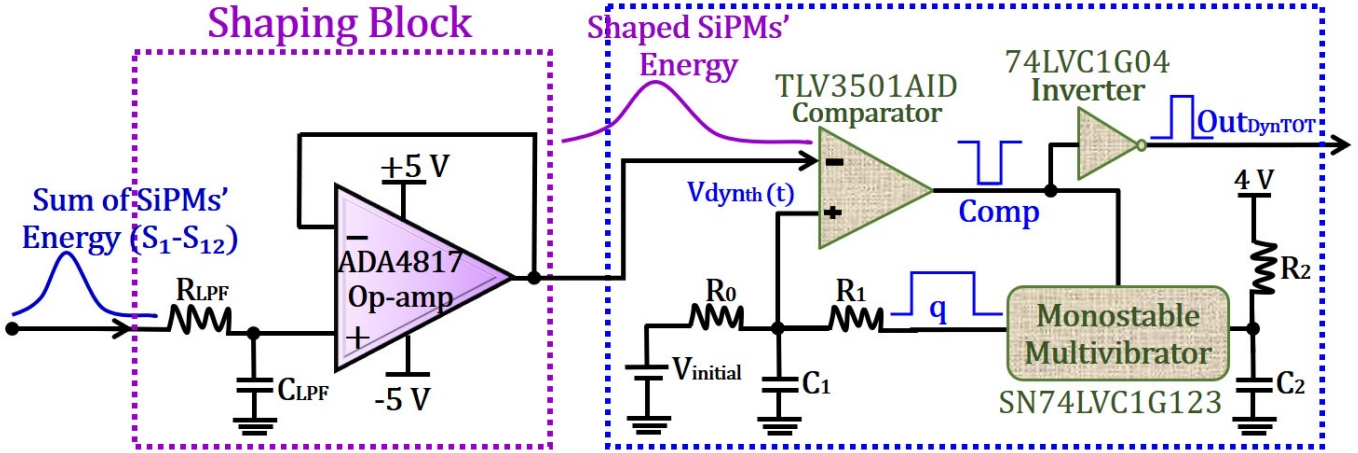


Using Dynamic TOT:

- To get excellent energy resolution
  - **Rejection of a higher fraction of scatter events**
  - **Reconstructing higher quality images**
- Extract information from Compton scatter events within the detector blocks
  - **Improve contrast of reconstructed PET images**

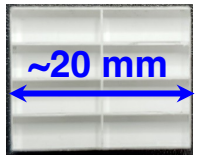


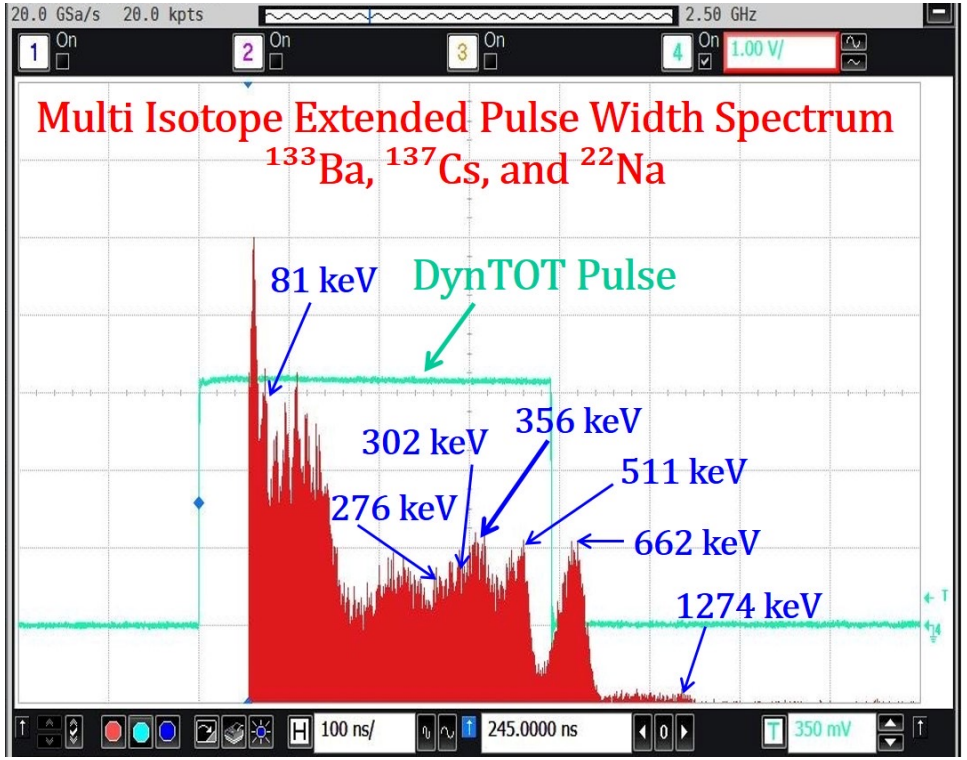
- Shaping block needed to **extend the DynTOT** pulses for being compatible with **625 ps resolution** FPGA-based multiphase counter **(MPCNT)** used to directly measure the energy

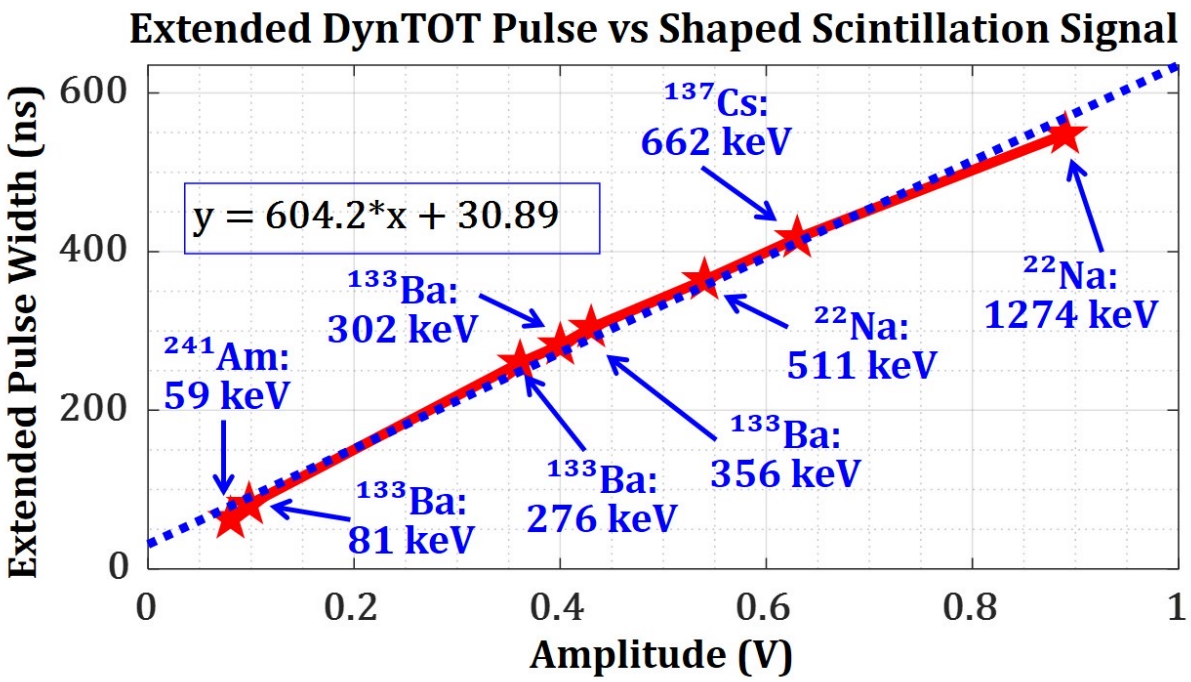


Energy Linearization & Wide Photon Detection Dynamic Range

- **Using 2x4 array of 3x3x10 mm³ fast LGSO crystal coated with $BaSO_4$ reflector**

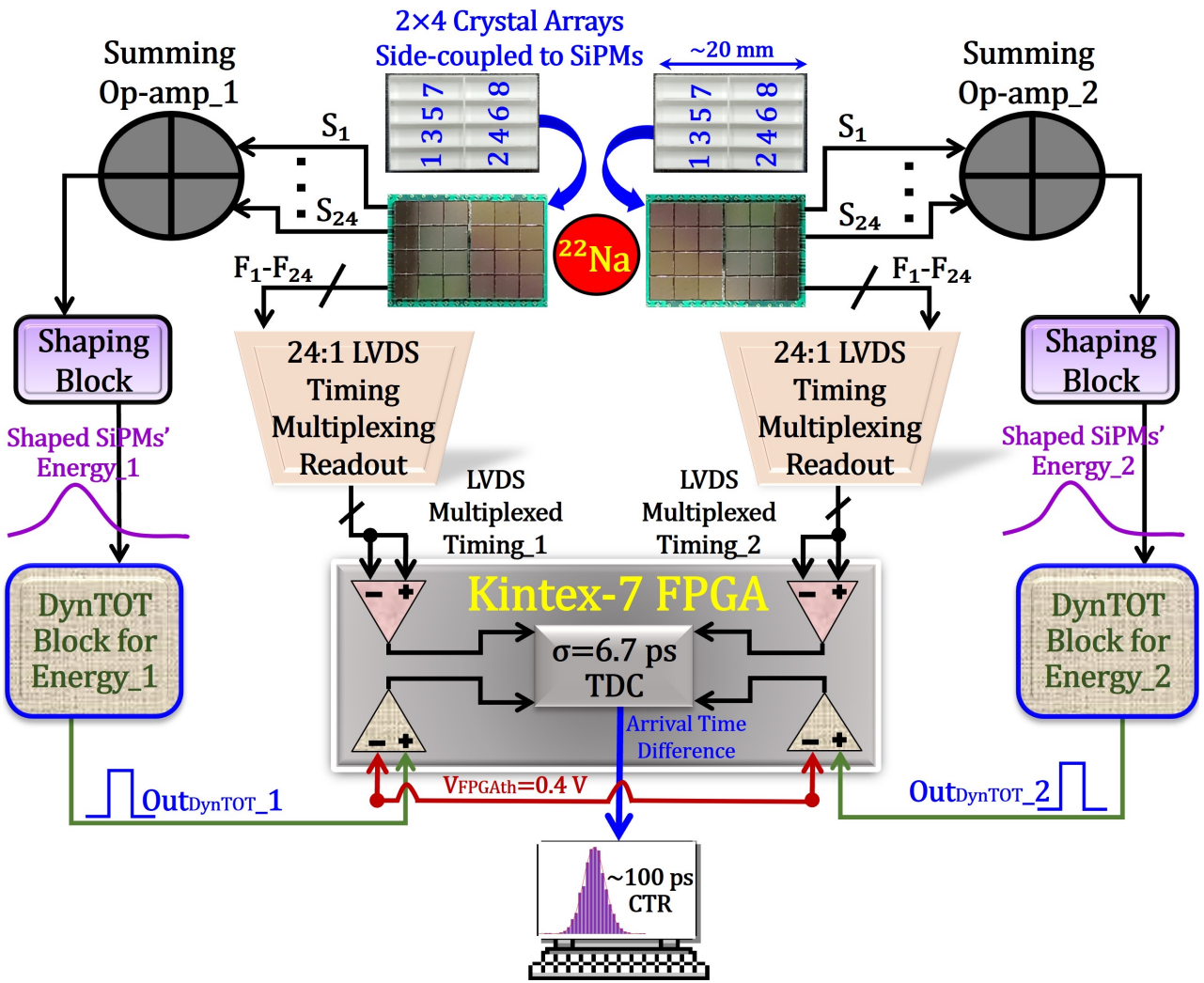






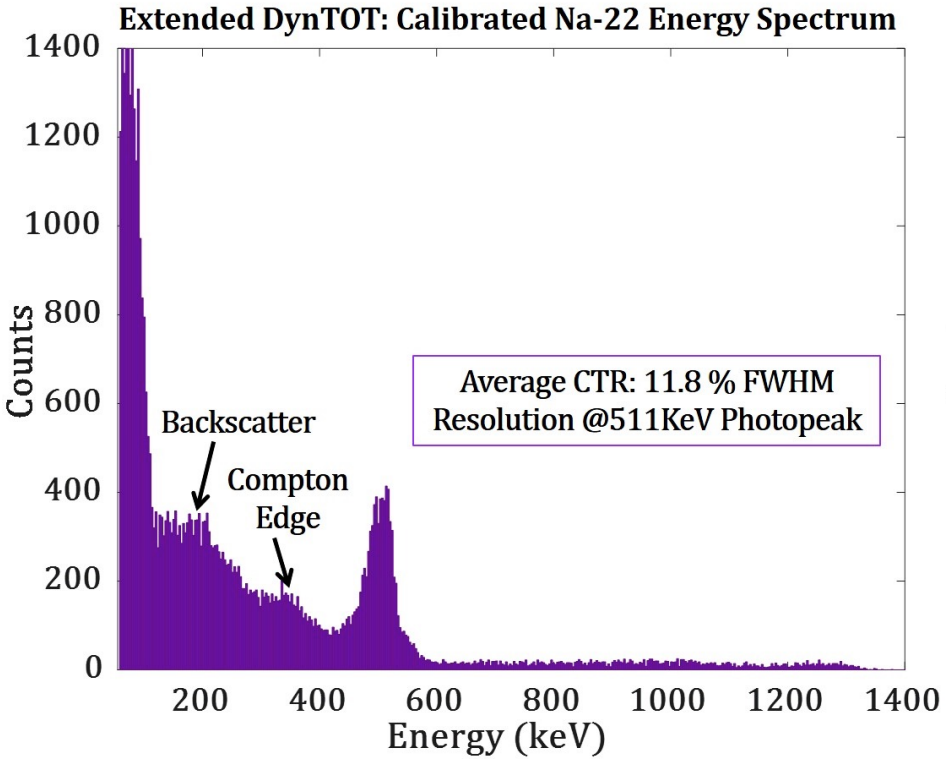
- Ability of resolving **59 keV energy** means recovering 511 keV photons that undergo Compton scatter within PET detector blocks at **angles as small as ~29°**

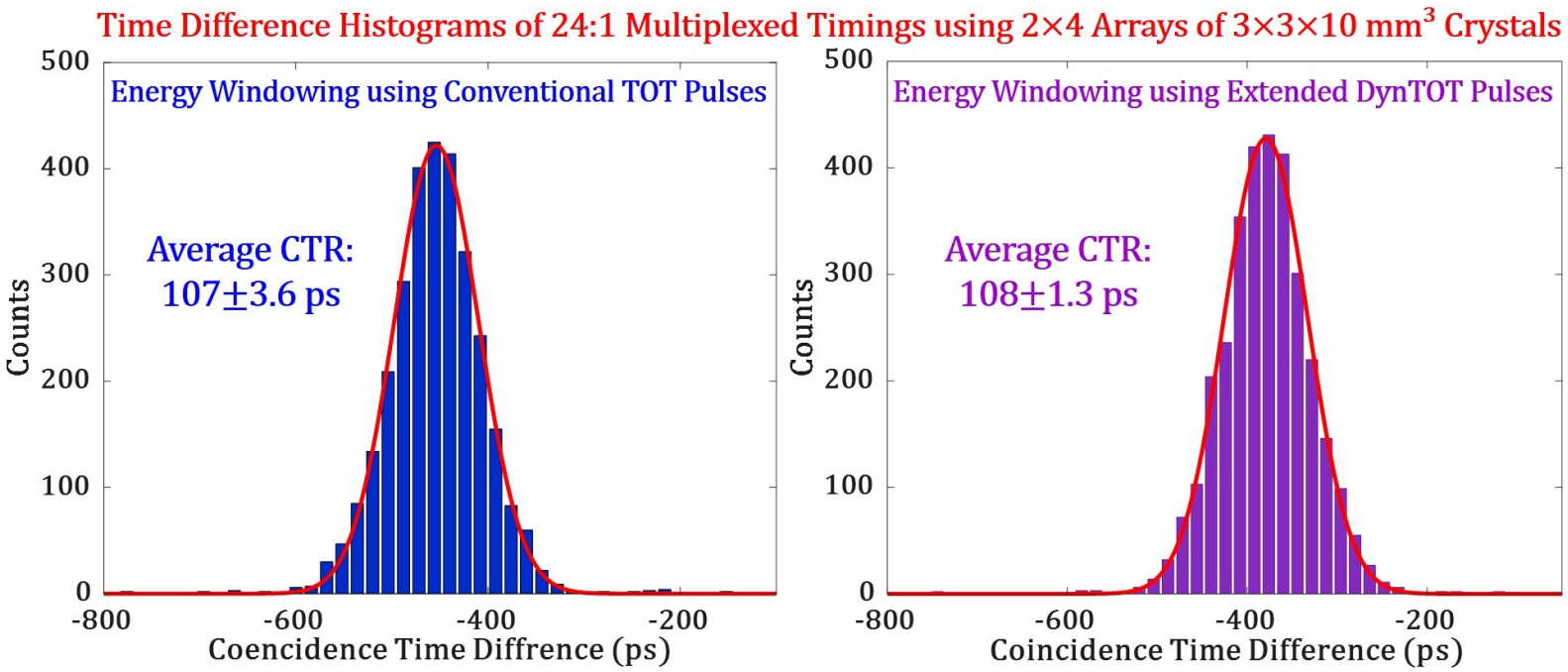
CTR Set-up Using DynTOT Blocks for Energy Gating



- Side-coupling 2x4 arrays of 3x3x10 mm³ fast LGSO crystals to 24 SiPMs (6x4 arrays)
- Using 24:1 timing multiplexing readouts
- **625 ps resolution** FPGA-based **MPCNT** used to directly measure the energy

ER & CTR Performance after Embedding DynTOT Block with Extended Pulses

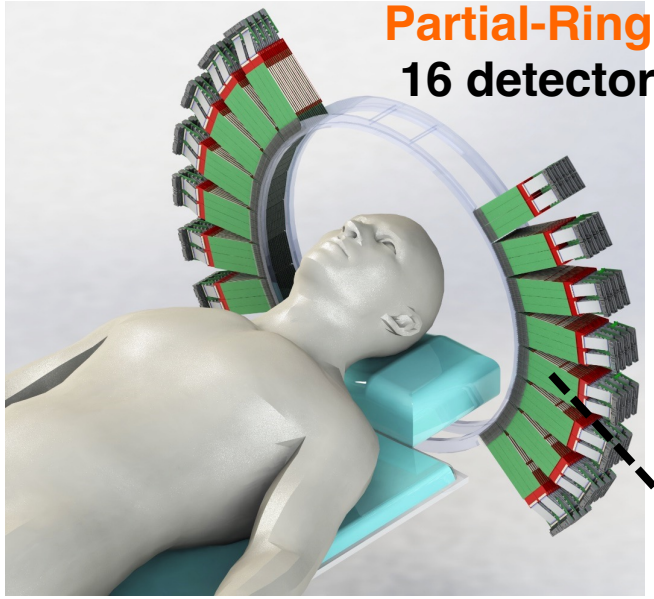


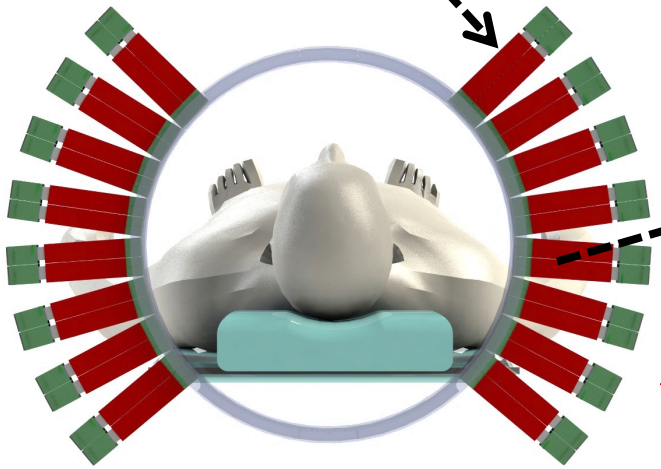


S. Pourashraf, *J. W. Cates*, and C. S. Levin, "A Scalable Dynamic TOT Circuit for a 100 ps TOF-PET Detector Design to Improve Energy Linearity and Dynamic Range", *IEEE Transaction on Radiation and Plasma Medical Sciences*, Dec. 2023. DOI: 10.1109/TRPMS.2023.3344399 2023.

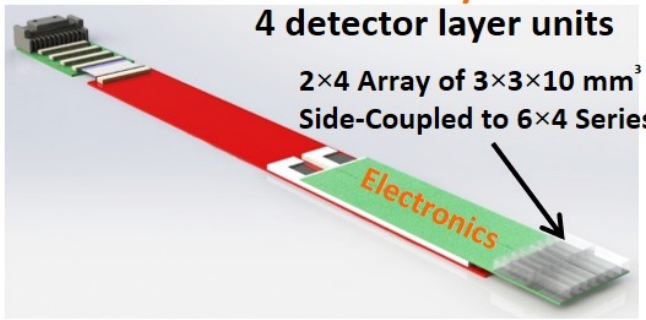
Scale-Up Procedure

- S. Pourashraf, et al, IEEE TRPMS, 2023
- S. Pourashraf, et al, IEEE TRPMS, 2022
- S. Pourashraf, et al, Physics in Medicine and Biology, 2021

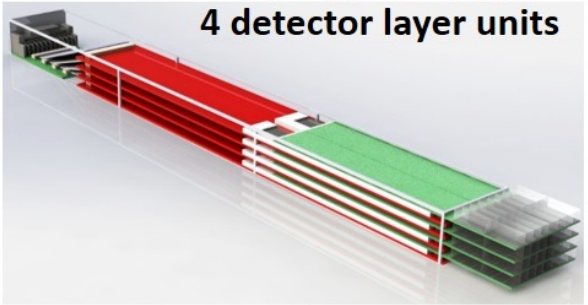




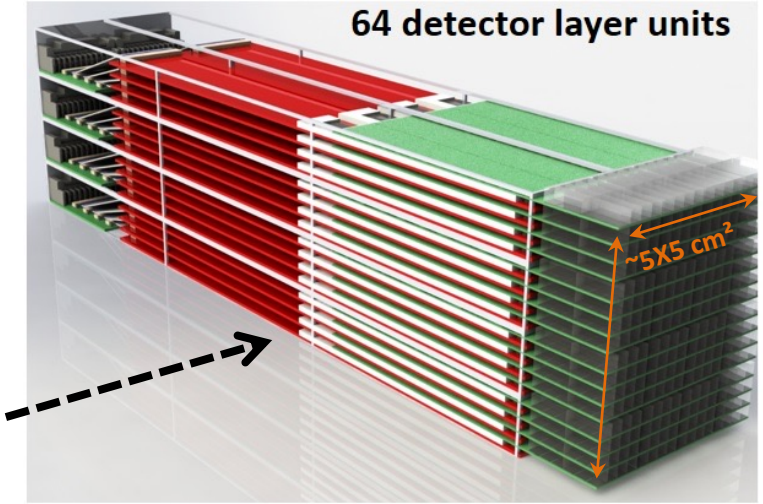
Detector Layer Unit:
4 detector layer units



Sub-Module Unit
4 detector layer units



Detector Module
64 detector layer units

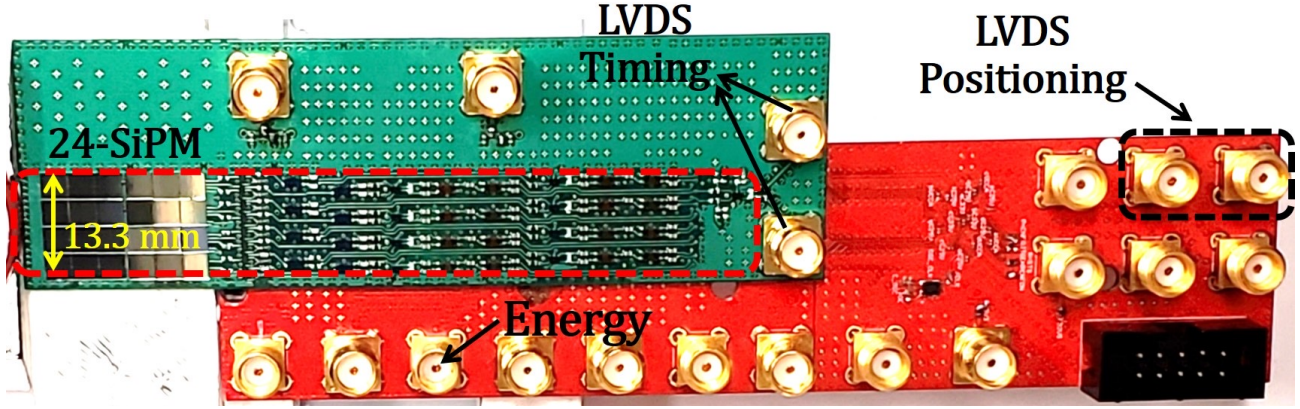


64 Timing

32 Energy

SMA-Less Detector Layer Units

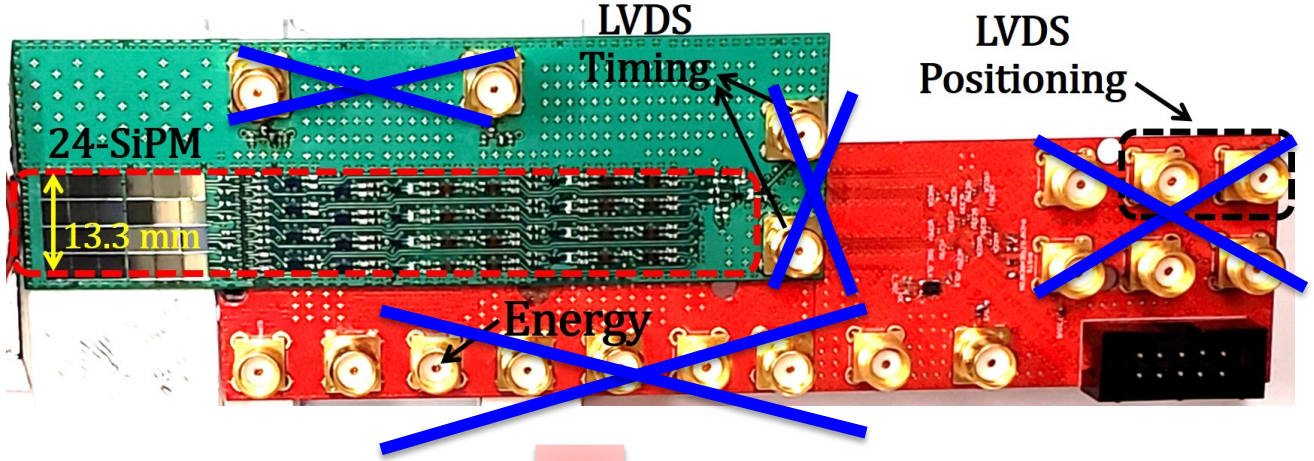
Previous Readouts with SMA Connectors

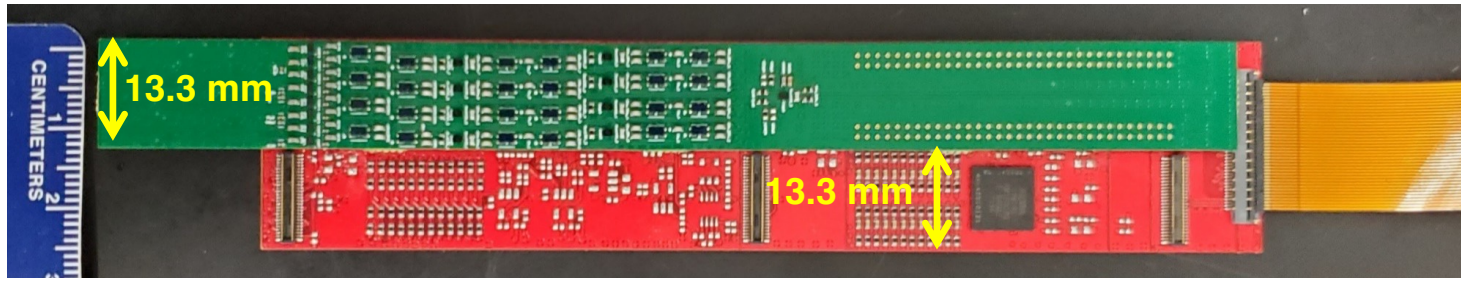


- Impossible to be used in System Level

SMA-Less Detector Layer Units

Readouts with/without SMA Connectors





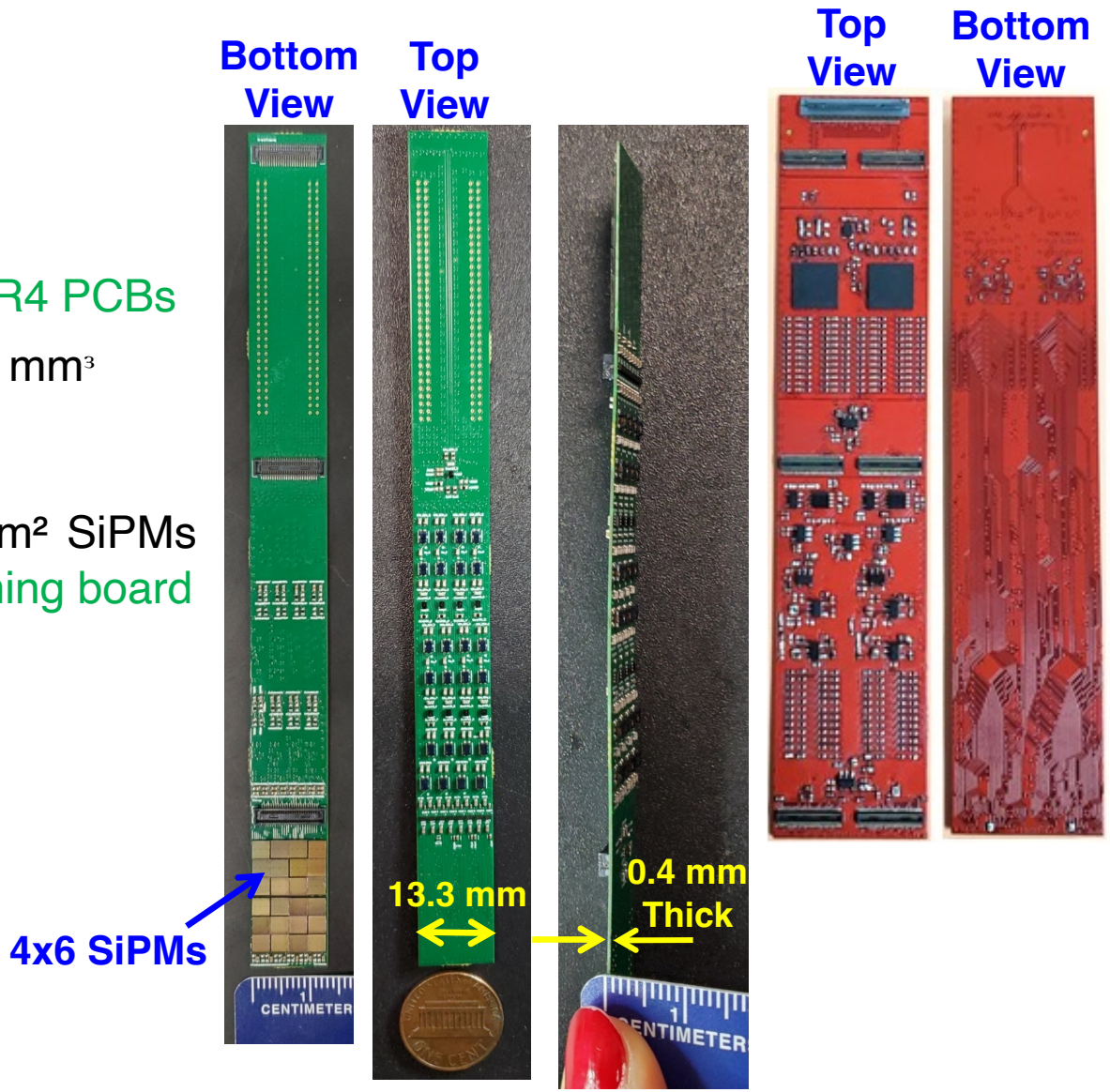
For system level implementation:

- Replacing bulky SMA connectors with low profile (~1.5 cm) connectors
  - All active/passive components are replaced with their low profile (less than 1.5 cm height) counterparts
- Merging each two detector layer units for maintenance ease and/or saving some resources/space/power dissipation

SMA-Less Detector Layer Units

- **Timing readout**
  - Green 4-layer FR4 PCBs
  - 13.3 x 147 x **0.4** mm³

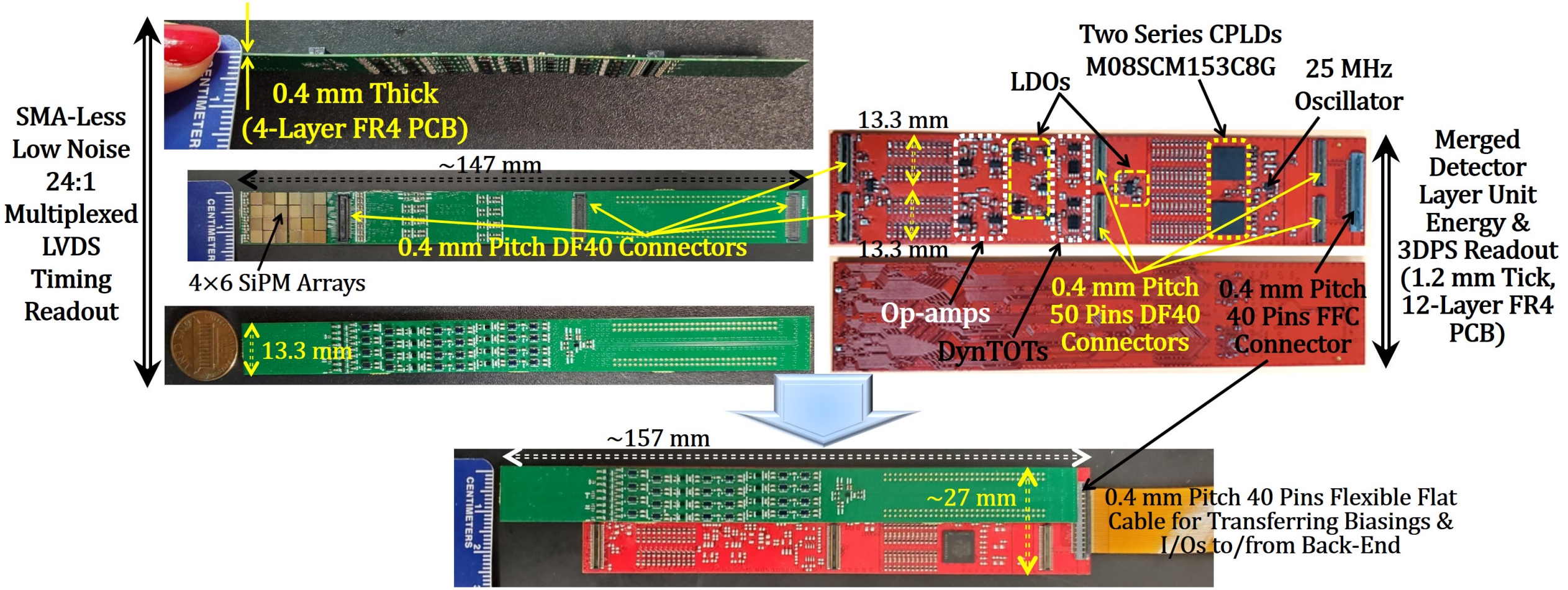
- 4x6 array of 3x3 mm² SiPMs on back of green timing board



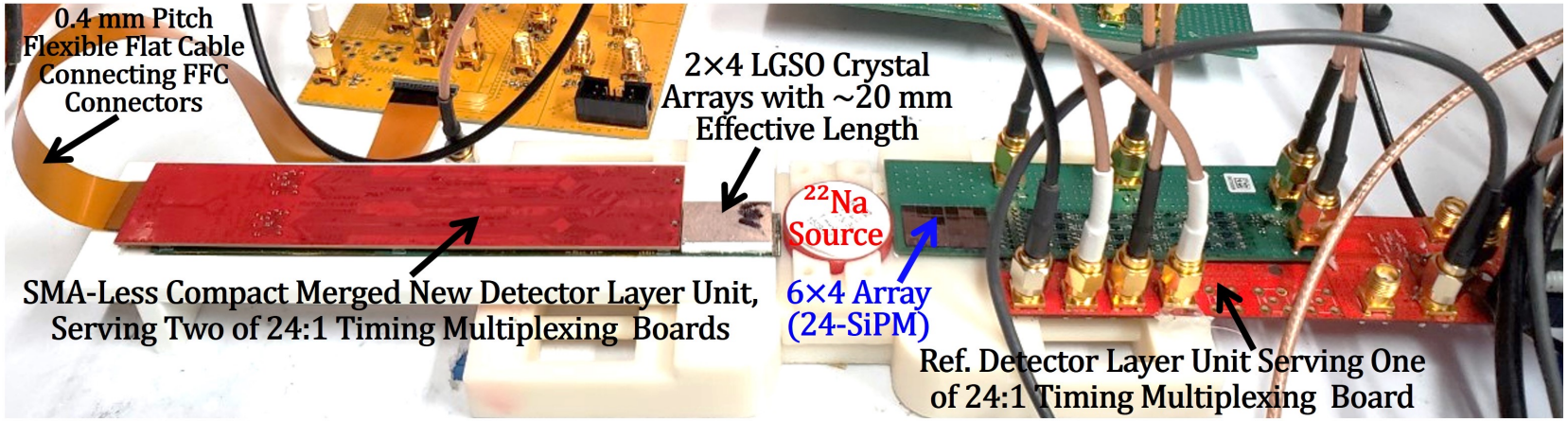
- **Energy/positioning readout or merged detector layer unit**
  - Red 12-layer FR4 PCB
  - 27.5 x 130 x **1.2** mm³

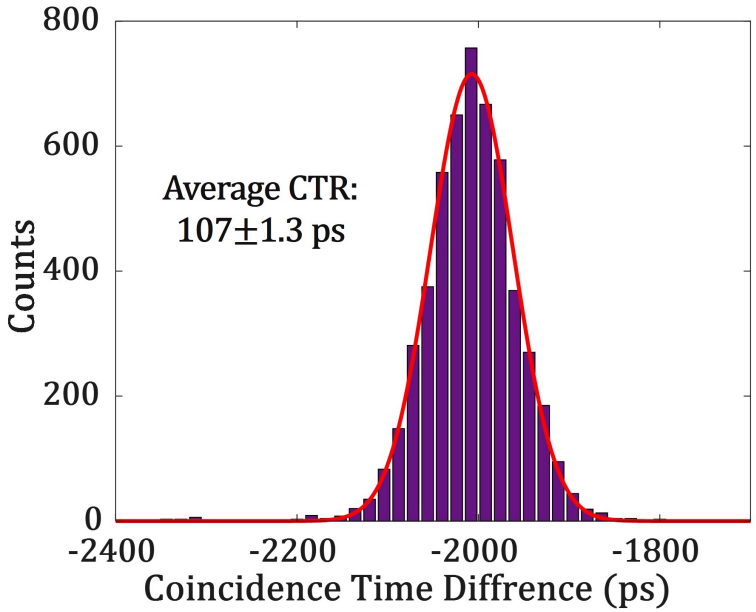
- Each two **timing boards** mounted on a merged detector layer unit board (**red PCB**)
  - Ease of maintenance

Details of SMA-Less Detector Layer Units



CTR Set-Up of Skinny Readout in Coincidence with Reference Detector

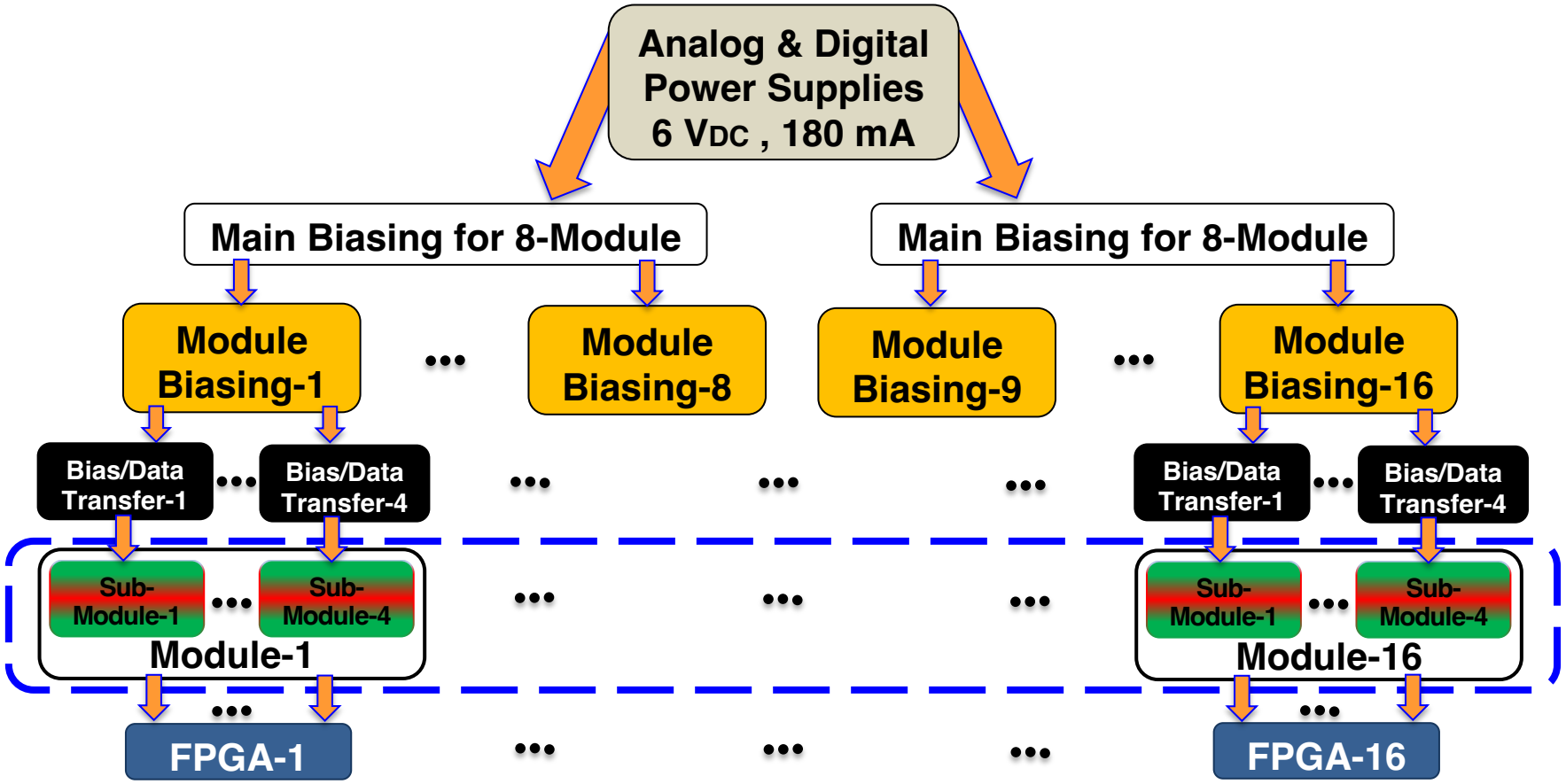




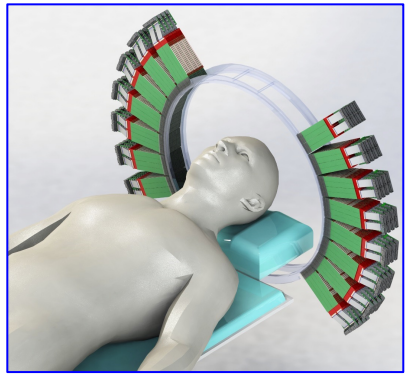
Screenshot of FPGA Logic Analyzer

- Comparable timing/energy signals of skinny and reference detectors
- CTR performance still kept at ~100 ps

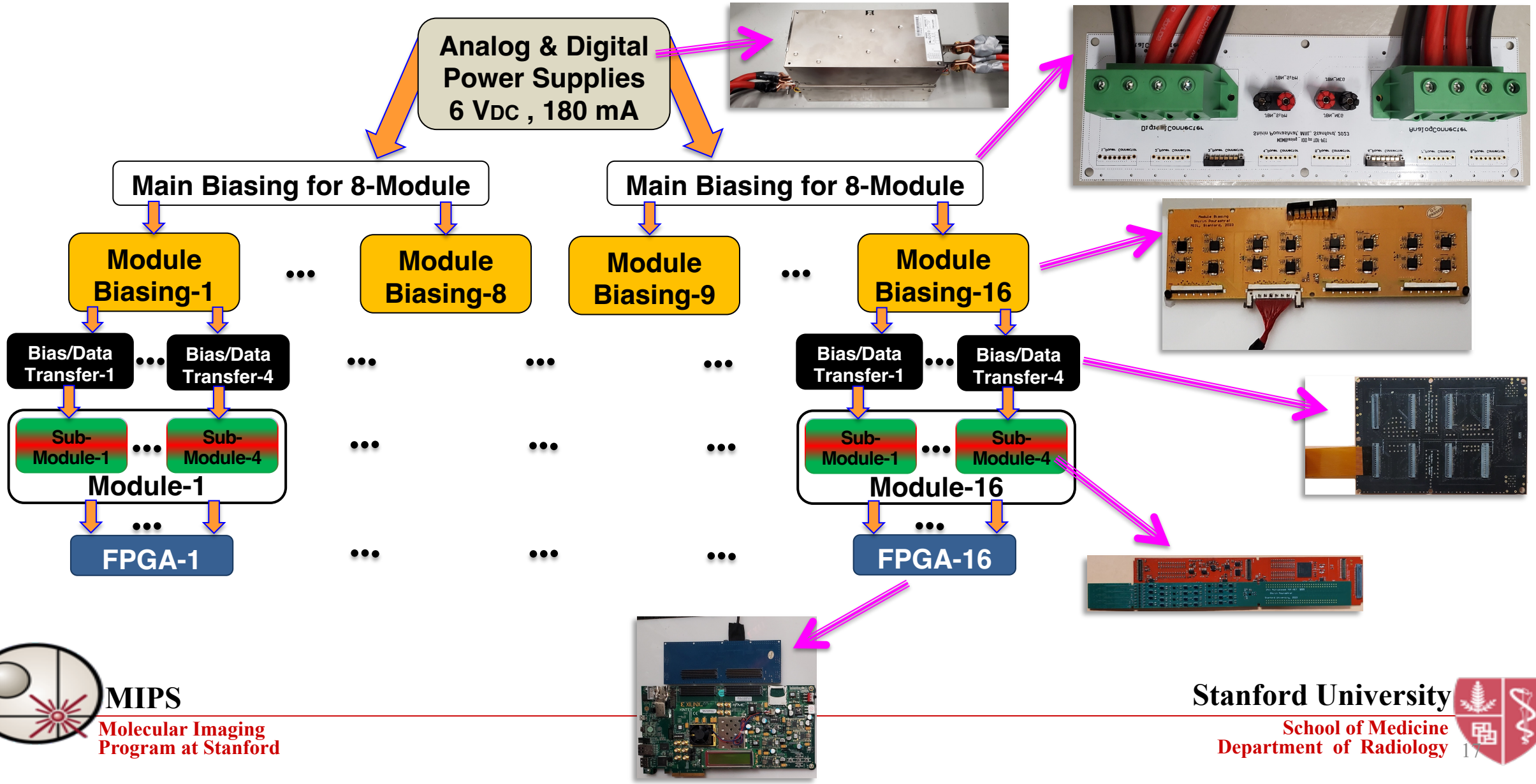
Overview of System Level Connectivity



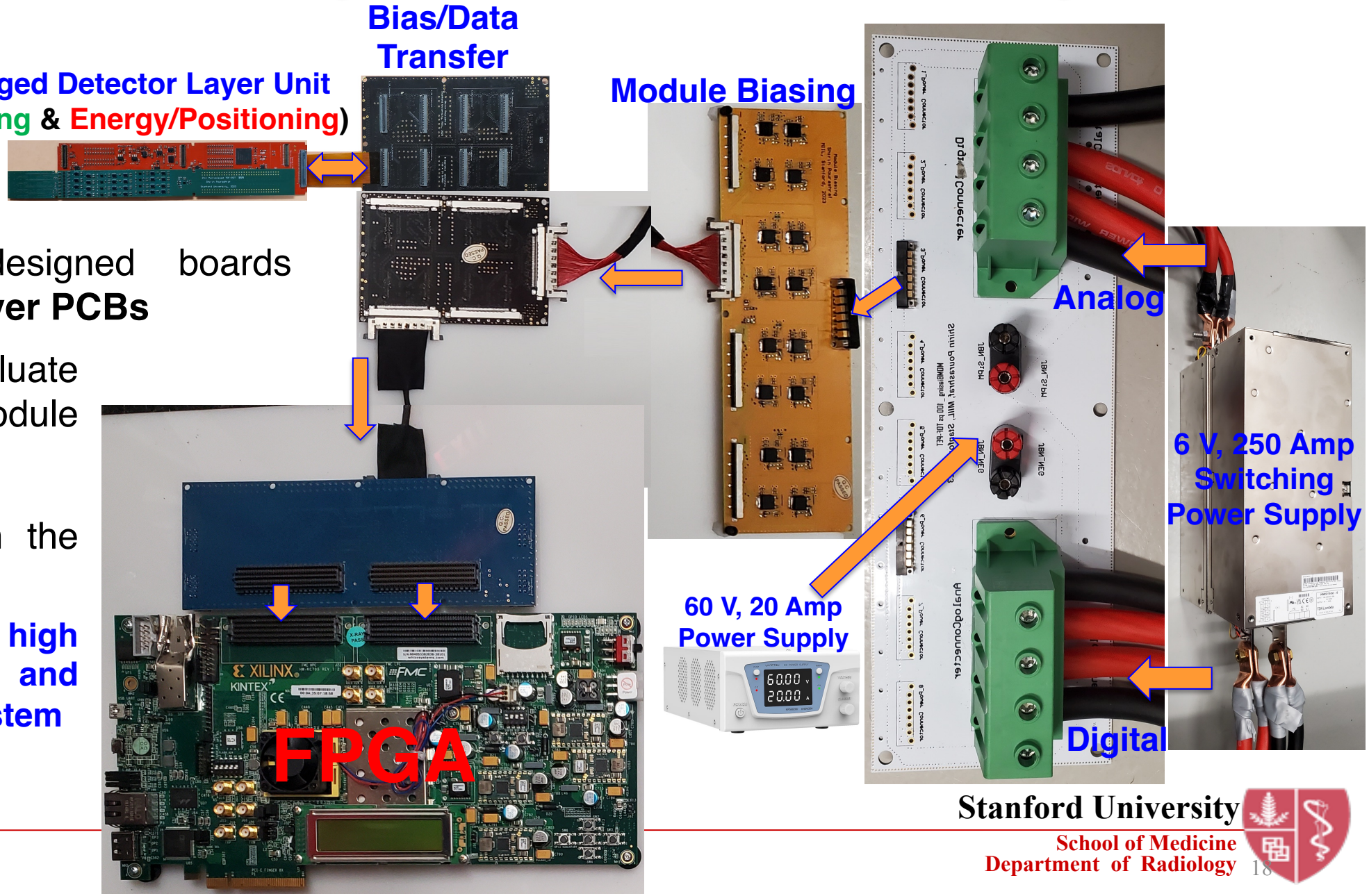
Partial-Ring TOF-PET: 16 Detector Modules



Overview of System Level Connectivity

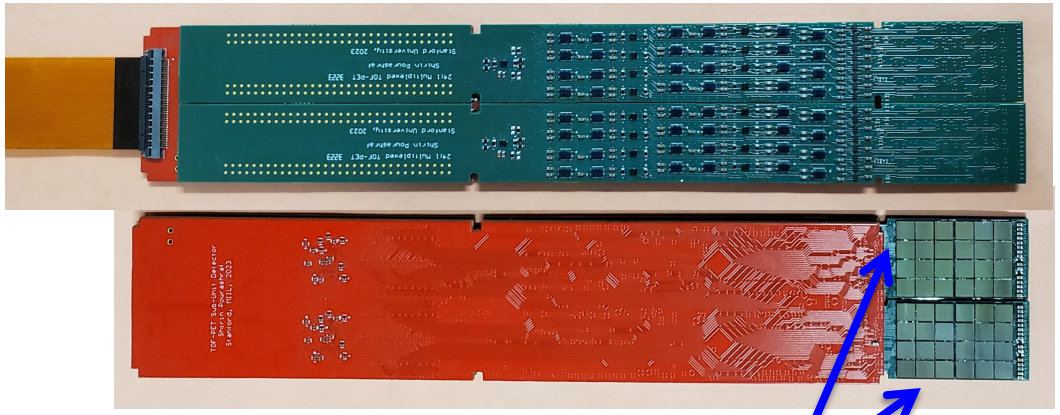


Real System Level Connectivity



- Low-noise custom-designed boards from **4-layer to 12-layer PCBs**
- Being used to evaluate the detector module performance
- Bulky boards are in the back-end
  - **Not affecting the high packing fraction and sensitivity of our system**

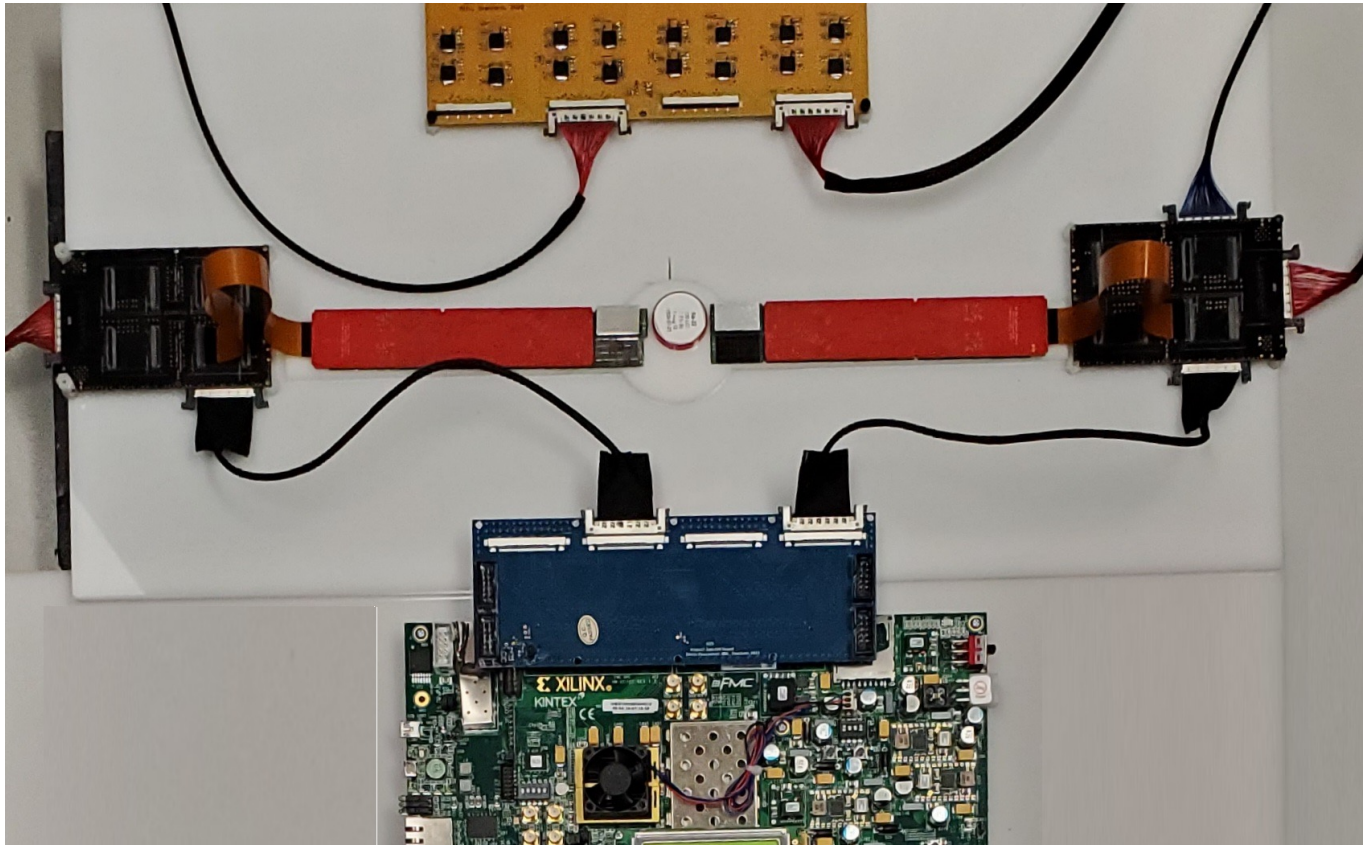
Physical Boards Arrangements



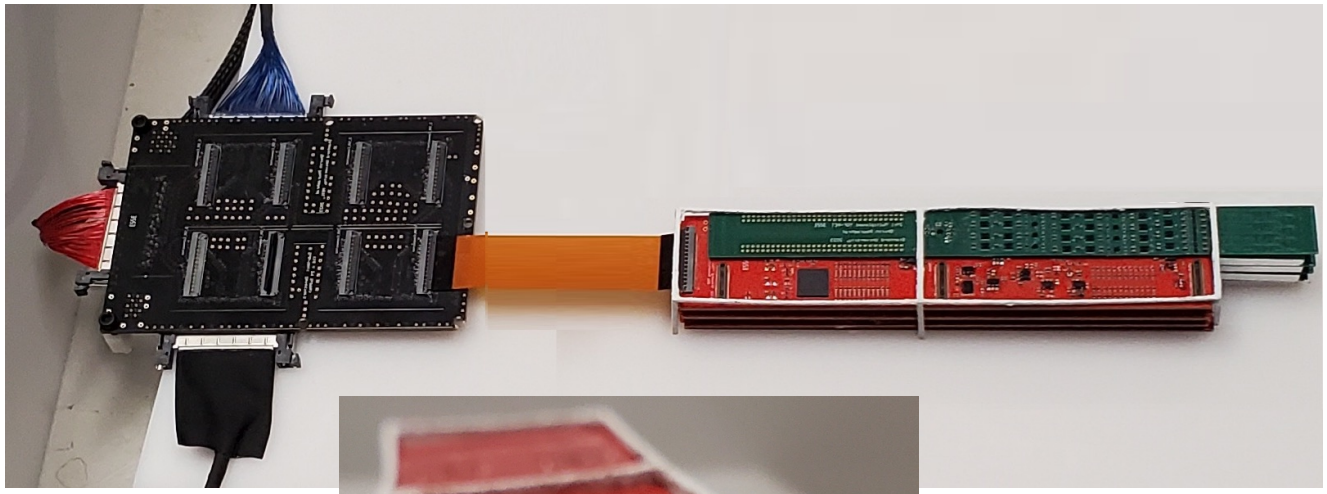
Two 4x6 arrays of SiPMs (24+24)

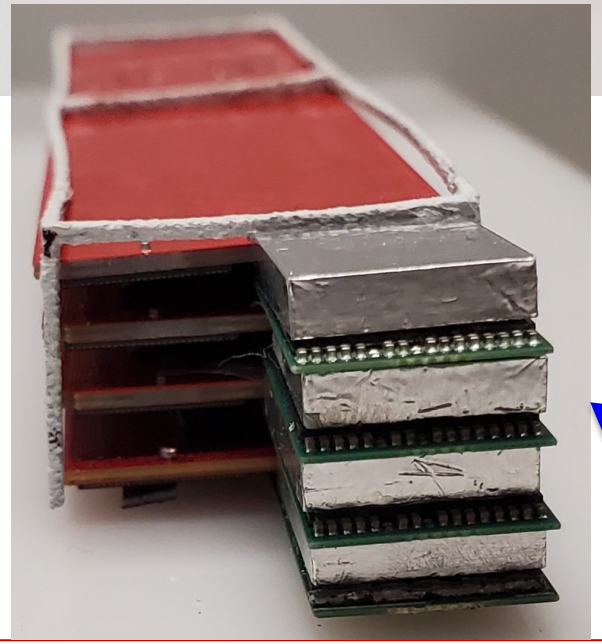
- Length/thickness/material of the interconnecting flex and multi-coax cables are going to be optimized to keep the **signal integrity** and **CTR performance**!

SMA-Less CTR Set-up

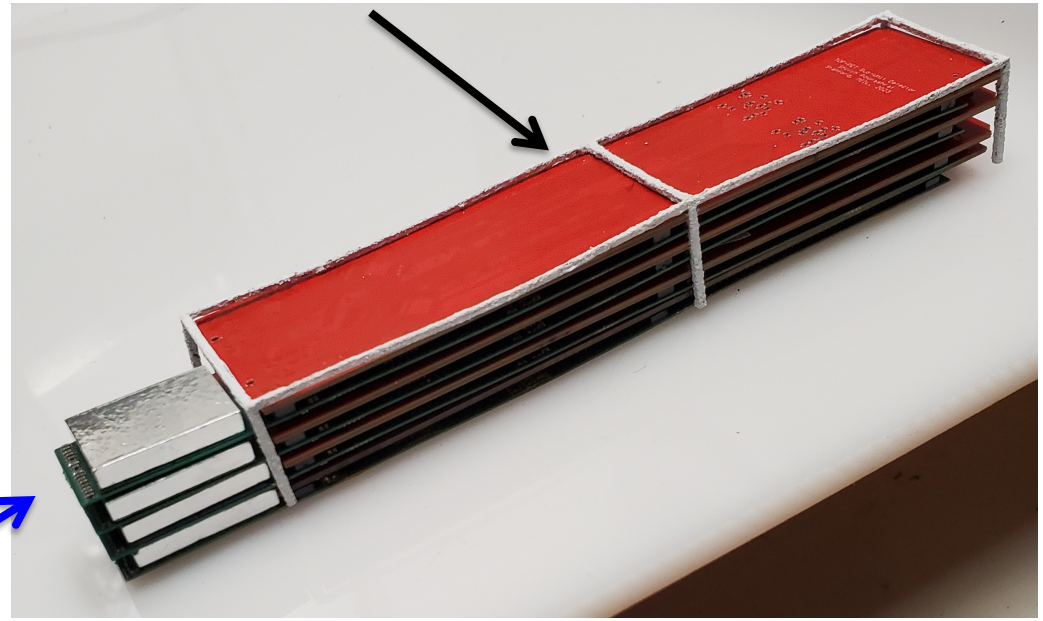


Stack of High Packing Fraction Detector Layer Units





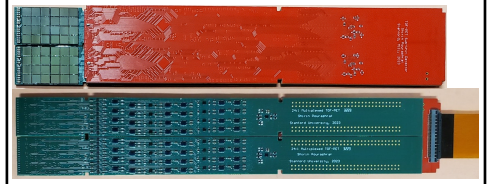
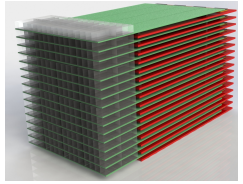
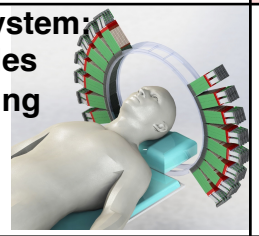
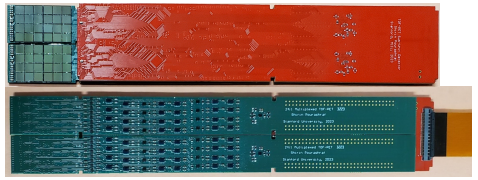
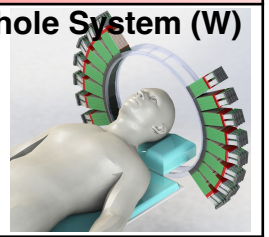
- ~1 mm thick mechanical holder to firmly keep the stack of skinny detector layer units within the module!
  - Still under further optimization



- Stack of 2x4 array of 3x3x10 mm³ fast LGSO crystals coated with $BaSO_4$ reflector

Resources & Power Consumption

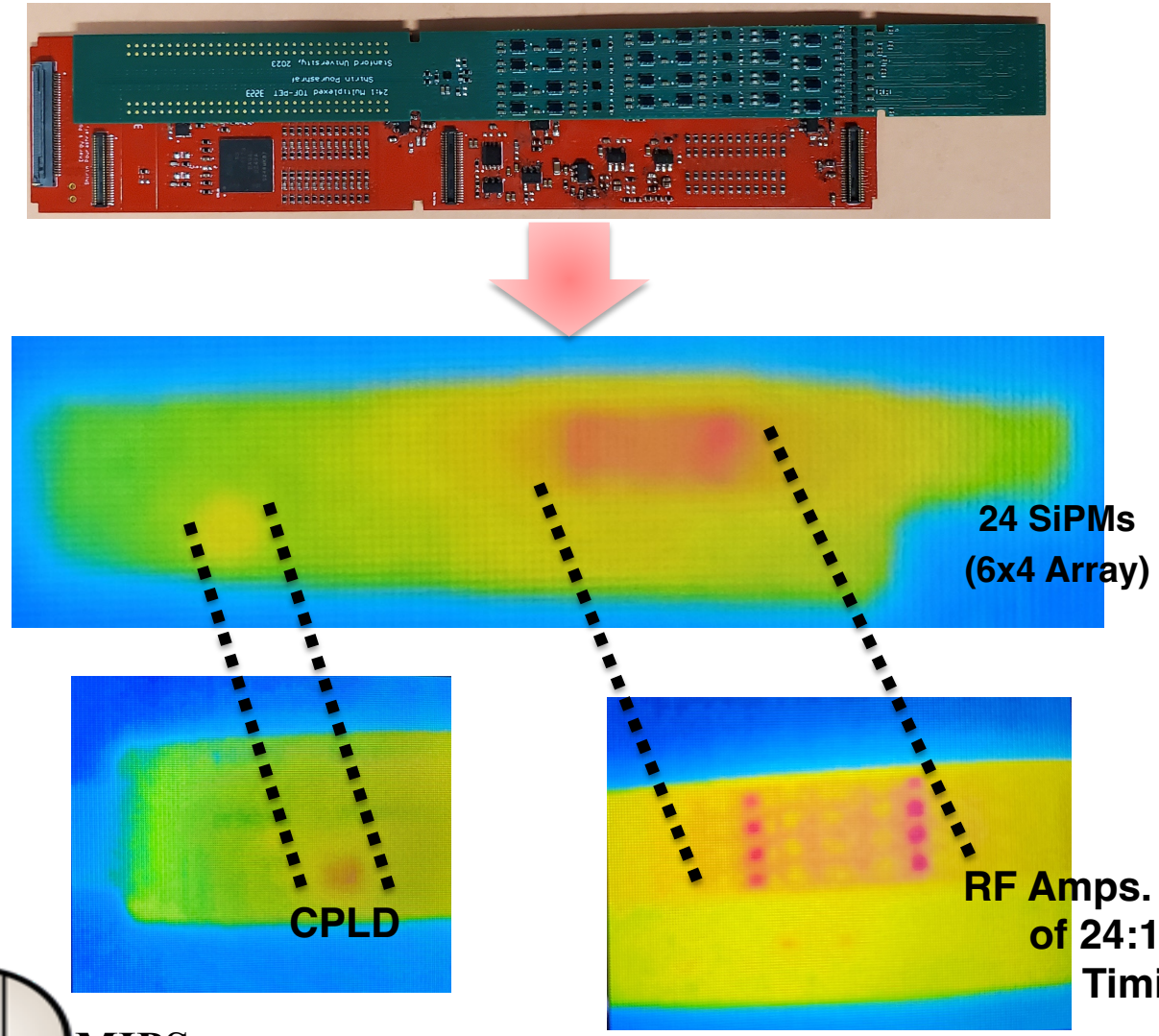
Detector Resources and Power Dissipation

	Resources Quantity			Power Dissipation	
	Merged Detector Layer Units 	Detector Module 	Whole System: 16-Modules Partial-Ring 	Merged Detector Layer Unit (mW) 	Whole System (W) 
2×4 Array of 3×3×10 mm³ Crystals	2 × 1	64	1024	-	-
SiPMs	2 × 24	1536	24576	3*	2*
LDO for Timing Comparators	2 × 0.5	32	512	1 × 135	69.1
Timing Comparators	2 × 9	576	9216	2 × 390	400
LDO for RF Amps.	2 × 0.5	32	512	1 × 52	26.6
RF Amps.	2 × 8	512	8192	2 × 145	148.5
LDOs for ±5 V of Op-amps	2	64	1024	2 × 11.5	11.8
Op-amps**	2 × 2	64	1024	2 × 115	117.8
DynTOT (Digital ICs)	2 × 1	64	1024	2 × 11	11.3
LDOs for 3.3 V & 2.5 V of CPLD	2	64	2048	130	66.6
CPLD	2 × 1	64	1024	2 × 420	430.1
FPGA Channels	2	64	1024	2 × 4	4.1
Total Power Consumption				~ 1.26 W	~ 1.3 kW

* Estimated Maximum power in the presence of high dose of FDG

** Replacing **ADA4817** Op-amps with **lower power/height OPA694** op-amps saving us **~450 mW (0.23 kw)** power dissipation per merged detector layer unit (whole system!)

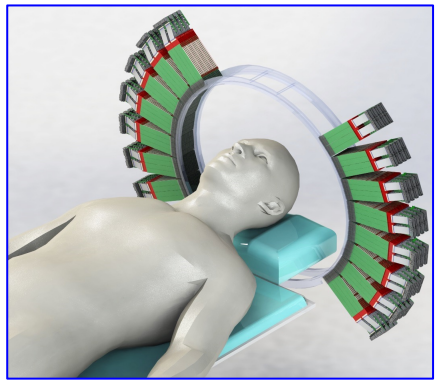
Thermal Imaging of Detector Layer Unit Readout



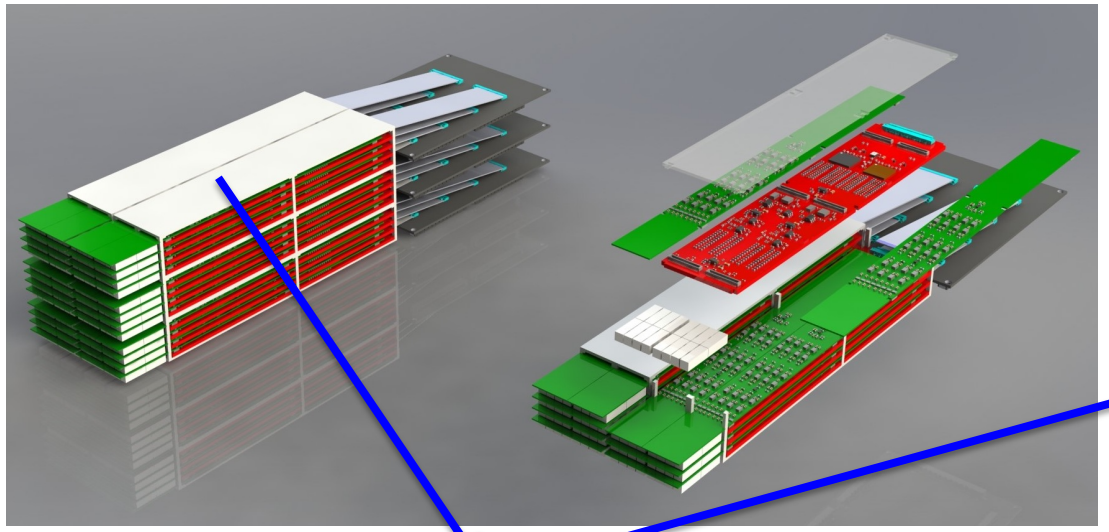
- Thermal imaging of merged detector layer unit (**red board**)
- Only one timing readout (**green board**) is mounted
  - **To see the heat spatial distribution (hot spots) of CPLD too**
- Images are used to embed an Effective Cooling System
  - **To push away the heat from the SiPM array and preserve their performance**

Detector Module Level Assembly

Partial-Ring TOF-PET:
16 Detector Modules



Front of Module



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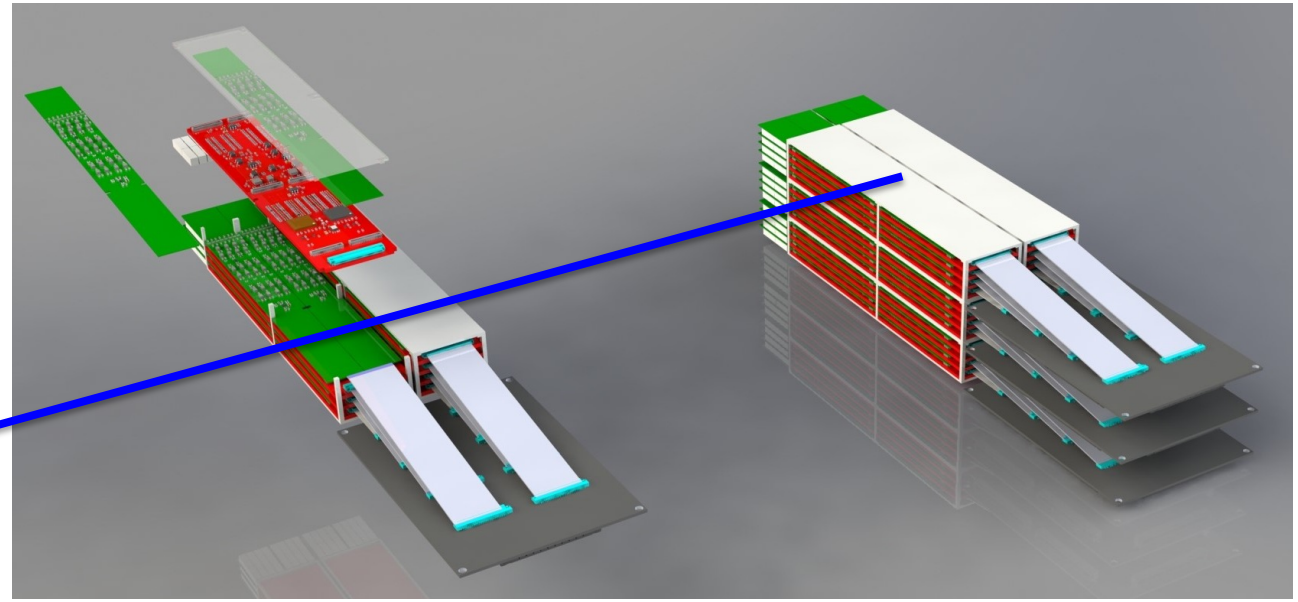
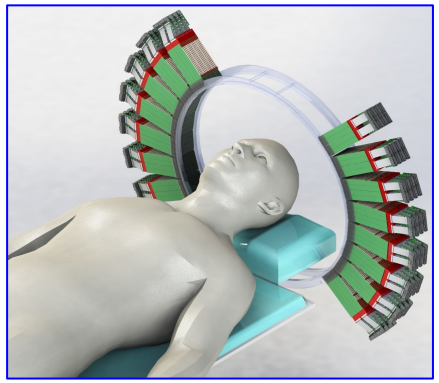


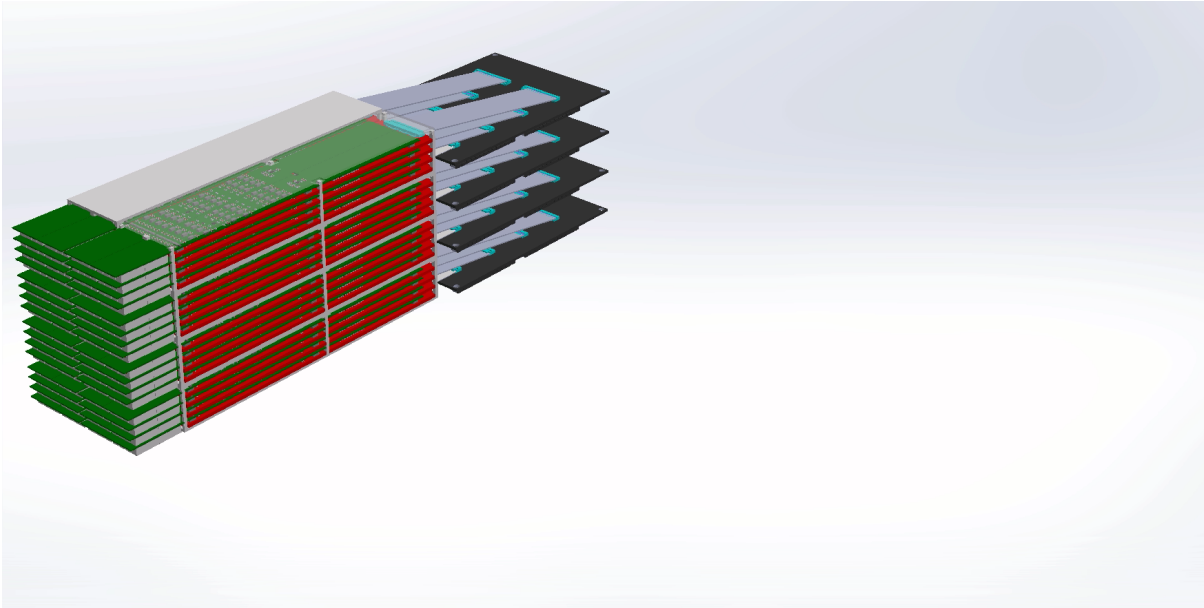
- White skinny sheets: thermal conductive materials to push away the heat from SiPMs outward

Detector Module Level Assembly

Partial-Ring TOF-PET:
16 Detector Modules



Front of Module



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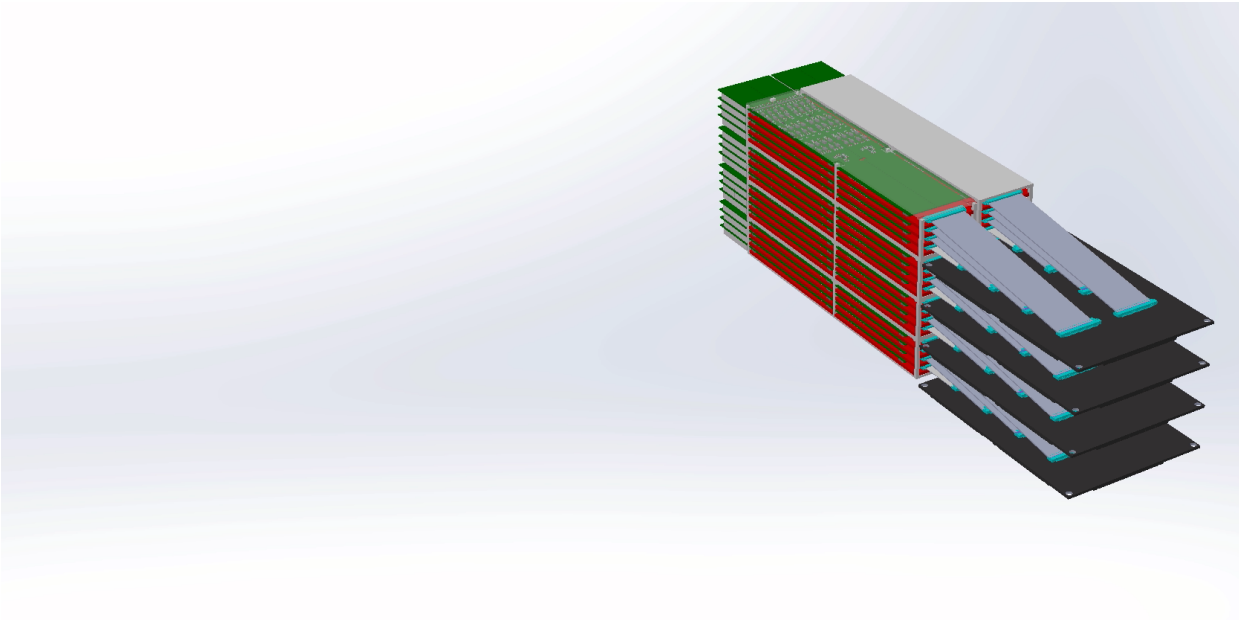
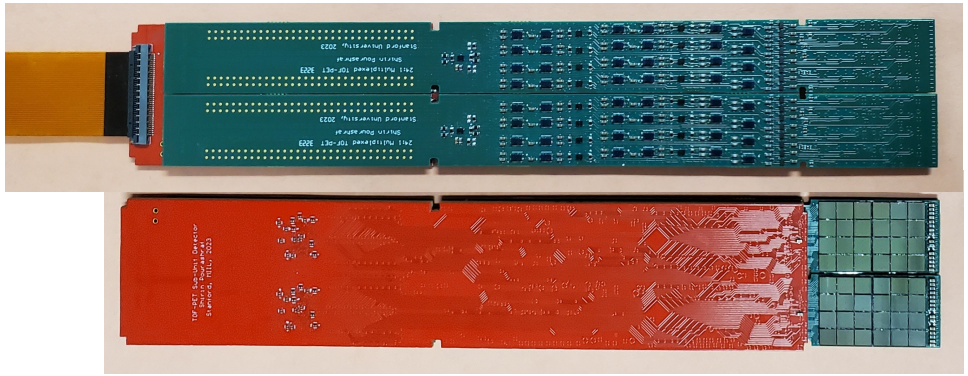
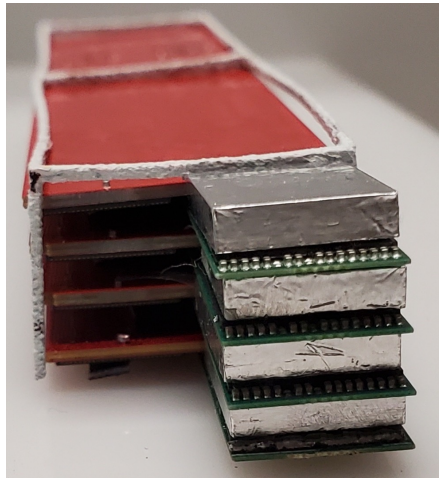


Discussion





- Finalized detector layer design and sub-modules
- Validated the performance of SMA-less skinny readouts
- Performing our thermal studies
- Evaluating sub-module/module detector layer units with multi-channel FPGA-based TDC

Acknowledgments

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Thanks!