

Technology development for a 100 picosecond coincidence time resolution time-of-flight positron emission tomography system

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Positron Emission Tomography (PET) System



• %80 of PET usage in Cancer:

- Detecting and staging specific types of cancer and/or assessing response to treatment
- Cardovascular and/or Neurollgical Disease
 - Evaluating the function of organs, such as the heart and/or brain



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- Positron emitter radionuclides
 e.g ¹¹C, ¹³N, ¹⁵O, & ¹⁸F
- Ring of Detector modules
 - Scintillation crystals + photosensor + electronic readout
- Event localization along lines of response (LOR)
 - Arrival time difference of coincident events



Time of Flight Positron Emission Tomography (TOF-PET)





- CTR (Coincidence Time Resolution): FWHM of Δt distribution
- D: Patient diameter (e.g. 40 cm)
- c = 3×10¹⁰ cm/s: speed of light
- Δx = c × CTR/2: Localization error

CTR (ps)	$\Delta x = c \times \frac{CTR}{2}$	$Gain = \frac{SNR_{TOF}}{SNR_{Non-TOF}} \approx \sqrt{\frac{D}{c \times \frac{CTR}{2}}}$
1000	15 cm	1.6
500	7.5 cm	3.1
400	6 cm	2.6
214	3.7 cm	3.5
100	1.5 cm	5.2



https://oncologymedicalphysics.com/nuclear-tomographic-imaging/



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State-of-the-Art: 214 ps CTR TOF-PET/CT





Single Bed Position Images



- Improved CTR (214 ps) and localization along LOR (3.7 cm)
 - Improved reconstructed image SNR, signal-to-background ratio, image quality, accuracy, and lesion detectability
- or getting the same image quality as Conventional PET
 - Lower injected dose to patients or shorter scan time
- **IIPS** Wider category of patients can be served

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System Level Electronic Readout for TOF-PET

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- At system level, 214 ps is the best commerciallyavailable CTR (Biograph TOF-PET/CT)
- Currently several benchtop experiments with CTR ≤100 ps using single-pixel detectors
 - Challenging to scale results up to full system

System Design Approaches:

- One-to-one coupling of scintillation crystals to compact sized SiPMs:
 - × Large number of electronic readout channels needed
 - × Costly, not power efficient, and heat generated degrading SiPM performance, especially CTR

- Designing ASICs
 - × Long design time
 - × Also costly



Multiplexing:

Simply hardwiring SiPMs signals together

× Parasitic capacitance >>> CTR degradation

- Resistive charge division × High RC constant >>> CTR degradation
- Delay-line method
- × Lower SNR, especially for longer delays
- × Requiring more resources from FPGA





Scale-Up Scheme of 100 ps TOF-PET Stanford Cancer Imaging

- J. W. Cates, C. S. Levin, Physics in Medicine and Biology, 2018
- S. Pourashraf, et al, Physics in Medicine and Biology, 2021
- S. Pourashraf, et al, IEEE TRPMS, 2022



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Multiplexing of Timing Channels



Why not simply combine LVDS signals?

• Standard LVDS has several advantages, but are current mode drivers not voltage!





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 Not aware of an electronic component to efficiently combine our sharp edge LVDS timings!



- But our case, several drivers (D) hanging off a main bus line with one receiver (R) at the end!
- Impedance mismatch and reflection due to stubs (unterminated length of drivers to the main bus)
- Needs careful considerations
 - Otherwise signal integrity issue, increased jitter, and loss of information



Our 24:1 Timing Multiplexing Approach





- Only passive micro-baluns and one extra comparator used
 - Saving footprint
 - Cost effective

Power efficient
Just 4.5 mW/Channel
extra power dissipation!

- Converting 8-LVDS timing signals to single-ended outputs using passive micro-baluns
- Then again converting these single-ended outputs to differential signals using micro-baluns
- Finally, hardwiring these 8 differential timing outputs at nodes A₁...₈ & B₁...₈ inputting the differential pins of the last MAX40025 comparator to produce the final LVDS timing channel



PCBs for System Development





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Compact and scalable

- Timing chain implemented in 13.3 mm width of a 4-layer FR4 PCB (green board)
- 4x6 array of 3x3 mm² SiPMs on timing board
- Energy chain implemented in 13.3 mm width of a 6-layer FR4 PCB board (red board)

PCB and Physical Implementation



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- Multiplexing chain:
 - Didn't increase the 13.3 mm width of our PCB 🙂
 - ✓ High sensitivity remains
 - Increased the length of PCB only ~27 mm
 - \checkmark Should not have effect on increasing jitter as the timing signals are already digitized! 🙂







Fail-Safe Biasing for Comparators



- External fail-safe resistive biasing at the differential inputs of all MAX40025 comparators
 - It provided 2.1 V common mode voltages for comparator's positive and negative inputs
 - It also provided V_{id}= 2.5 mV dropped on 82 Ω line termination resistors of comparator to clean up the LVDS timing signals at idle line states



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 Careful selection of resistive network is needed as it can introduce more jitter

 In our system, V_{id} can be <2.5 mV as the noise level is very low (~1 mV)





Experiments with 24:1 Timing Multiplexing Readout

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- LVDS 24:1 multiplexed timing signals of one detector unit (**Positive & Negative**)
 - Using 2x4 array of 3x3x10 mm³ fast LGSO crystal coated with BaSO₄ reflector
 - Triggered with Energy Signal







- Combined 24 SiPMs' fast output
 - 24:1 SiPM-to-channel multiplexing
- Average CTR of **107±3.6 ps** over multiple measurements @optimum 31 V SiPM biasing

– Near to 100 ps CTR as single 10 mm crystal detector ③







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- This 24:1 timing multiplexing method also has the potential to be used in other TOF applications due to:
 - -Simplicity and Scalability
 - -Cost/Area/Power Efficiency



-Most importantly, its "Ease of Implementation" & "Robustness"



Discussion



- Effective implementation of compact TOF-PET detector layer
 - Combined 8-timing channels (24 SiPM's fast outputs)
 - 107 ps FWHM CTR for 20 mm long crystal elements
 - 1.1 W power dissipation per detector unit layer
- Simpler possible version of the multiplexing scheme
 - Should mostly perform the same
 - Saving 7 micro-baluns
- There is a high potential this multiplexing scheme can serve more than 24 SiPMs (e.g. 48)





Next Steps:

Bottom

View

• **Currently** testing SMA-less Detector Layer Units (highly compact)

> 0.4 mm DF40C connectors

- Timing measurements with green 4-layer FR4 PCBs of 13.3 mm width & 0.4 mm thickness
- 4x6 array of 3x3 mm² SiPMs (photo-sensors) on back of green timing board

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4x6 SiPMs



Previous Readout with SMA Connectors



Under Test SMA-less Readout (Challenging to test)



• Each two timing boards will be mounted on a **10-layer FR4 red board** assigned for energy and positioning assessment



Getting Closer to Final Goal: Partial-Ring TOF-PET (16 Detector Modules)











Thank You! and

Mentors:

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Stanford MEDICINE Molecular Imaging Instrumentation Laboratory



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