An RF-Ultrasound Relay for Adaptive Wireless Powering Across Tissue Interfaces

Ernest So\textsuperscript{\textregistered}, Graduate Student Member, IEEE, Pyungwoo Yeon\textsuperscript{\textregistered}, Member, IEEE, E. J. Chichilnisky\textsuperscript{\textregistered}, Member, IEEE, and Amin Arbabian, Senior Member, IEEE

Abstract—Single modality wireless power transfer has limited depth for mm-sized implants across air/tissue or skull/tissue interfaces because they either suffer from a high loss in tissue (RF, optical) or high reflection at the medium interface [ultrasound (US)]. This article proposes an RF-US relay chip at the media interface avoiding the reflection at the boundary and enables efficient wireless powering to mm-sized deep implants across multiple media. The relay chip rectifies the incoming RF power through an 85.5\% efficient RF inductive link (across air) using a multi-output regulating rectifier (MORR) with 81\% power conversion efficiency (PCE) at 186 mW load and transmits using adiabatic power amplifiers (PAs) to the implant in order to minimize cascaded power loss. To adapt US focus to implant movement or placement, beamforming was implemented using six channels of US PAs with two-bit phase control (0°, 90°, 180°, and 270°) and three different amplitudes (6–29, 4.5, and 1.8 V) from the MORR. The adiabatic PA contributes a 30\%–40\% increase in efficiency over class-D and beamforming increases the efficiency by 251\% at 2.5 cm over fixed focusing. The proof-of-concept powering system for a retinal implant, from an external PA on a pair of glasses to a hydrophone with 1.2 cm (air) + 2.9 cm (agar eyeball phantom in mineral oil) separation distance, had a power delivered to the load (PDL) of 946 \(\mu\)W. The 2.3 mm \(\times\) 2 mm relay chip was fabricated in a 180 nm high-voltage (HV) BCD process.

Index Terms—Adiabatic power amplifier (PA), beamforming, implantable medical device (IMD), in-depth powering, inductive powering, multi-output regulating rectifier (MORR), phased array, power relay, retinal implant, ultrasonic power transfer, wireless power transfer.

I. INTRODUCTION

Implantable medical devices (IMDs) are a promising approach for treating a variety of disorders including paralysis [1]–[3], stroke [3], epilepsy [4], and vision loss [5]–[7] due to their ability to interface with high specificity within tissue. Modern IMDs use wires and large bulky batteries which can cause tissue damage and infection [8]–[10]. Recent research has been aimed to miniaturize IMDs and reduce power to alleviate these complications, which has enabled wireless powering solutions [11]–[16].

Wireless powering has a few distinct advantages for mm-sized IMDs. Compared to bulky battery solutions, the implant can be further miniaturized with small transducers. The longevity of the device can be extended since it is no longer limited by battery life. Eliminating the wire mitigates the risk of infections and also helps simplify the surgery [17].

Current wireless powered IMDs are either powered by RF, optical (light), or ultrasound (US). Each modality has its own advantages and disadvantages. Near-field RF has high efficiency when the transducer size is comparable to the separation distance and minimally interacts with tissue, making it good for shallow implants that are under layers of heterogeneous material such as neural implants [18], [19]. Optical has the potential for extreme miniaturization since the wavelength is extremely small and the receivers (Rx) can be integrated on-chip [20]. However, scattering in tissue limits the implant depth in most applications except the eye. US has favorable properties including low-loss propagation [21], [22], high allowed power intensity [23], and good transducer coupling due to mm wavelengths [14]. Because of these reasons, US has been used for powering IMDs for various sensing applications including blood pressure [24], imaging [25], electrochemical sensing [26], [27], and neural recording [15], [28], [29]. However, it has high loss at the interface between air and tissue or bone and tissue [30].

Some implant applications require that the power be transferred across multiple media. When the difference in impedance between various media becomes large, there is a significant loss at the interface due to reflections. For example, power must pass through the skull and then brain tissue for powering neural implants, and then through the air and then the eye for retinal implants. For US, the difference in acoustic impedance for the above examples is large, resulting in almost all of the power being reflected [30]. This becomes critical when the wireless link must be efficient to supply power near the safety limits (few mWs). This is the case for the future brain–machine interfaces (BMIs) which seek to interact with the brain or retina with high resolution and large scale, and therefore the power must be high to maximize channel count [31], [32].

To pave the way for these future BMIs that have requirements of millimeter-sized, cm depth across multiple media, and mWs of power, new wireless powering solutions are...
needed. Single modality solutions are limited: RF and optical cannot power at depth with high power and US has a large interface loss due to acoustic impedance mismatch across multiple media.

This article is an extension of the work described in [33]. We expand on this work with additional circuit descriptions, analysis of the adiabatic power amplifier (PA) operation, and new measurements including the XY plane acoustic beamforming and a new ex vivo wireless power transmission experiment through a pig eye.

The article is organized as follows. In Section II, we propose an RF-US relay system with beamforming capability to address the challenges of wirelessly powering deep implants across interfaces between different mediums and describe considerations for the RF inductive link, rectifier, and US link. Section III dives into detailed circuit descriptions and analysis of the rectifier, power management unit (PMU), and US PAs. The system performance is characterized in Section IV with measurements of the rectifier, US PAs, acoustic link, and full end-to-end wireless link. Finally, Section V concludes and compares the RF-US relay system to state-of-the-art implant wireless power systems.

II. PROPOSED SYSTEM ARCHITECTURE

Our proposed solution to power mm-sized implants at cm depth across multiple media is to utilize the strengths of both RF and US similar to [30]. A cm-sized relay, as shown in Fig. 1, is placed at the interface of the two media around 1 cm deep and converts incoming RF power to US power. The RF inductive link can transmit power efficiently across the cm air or skull layer, and US can be focused on deep mm-sized implants in the tissue. The relay, which comprises an Rx coil, relay chip, and piezoelectric array, converts the received RF power to direct current (DC) electrical power on the chip and then converts the electrical power to US via PAs and the piezo array.

By converting RF to DC and then US instead of directly to US [30], we can control the amplitude and phase of each piezo element, fundamentally enabling dynamic control and programmability of the transmitted power in space through beamforming. Beamforming is critical for powering IMDs because the tissue can move, the implant can move within the tissue, or the surgical placement can be inaccurate.

In addition to assisting with beamforming, amplitude control enables power transmission control. For implants that are closer, farther away, or require different power levels, the transmitted power needs to be adjusted accordingly. For this, multiple voltage supplies are needed. Specifically, a dynamic high-voltage (HV) supply is needed to cover the dynamic range of cm variation and power requirements ranging from μWs to mWs.

Although the relay architecture takes advantage of the strengths of RF and US, adding a relay inherently adds a cascaded power loss that must be minimized to avoid degrading the system efficiency to performance comparable to single modality solutions. The efficiency of each piece, shown in Fig. 1(d), is optimized in order to minimize this loss. The system efficiency is given by

\[ \eta_{\text{system}} = \eta_{\text{RF-Inductive-Link}} \times \eta_{\text{PCE}} \times \eta_{\text{US-Link}} \]  

\[ \eta_{\text{PCE}} = \eta_{\text{Rect}} \times \eta_{\text{Reg}} \times \eta_{\text{US-PA}} \]  

where the power conversion efficiency (PCE) of the relay comprises of the rectification of the RF signal, voltage regulation, and conversion to power.

In Sections II-A–II-C, we will discuss the optimization and design decisions for the RF inductive link, multi-output regulating rectifier (MORR) that generates the multiple supply voltages, adiabatic PA, and US beamforming.

A. RF Inductive Link Design

The first piece of the system efficiency to optimize is the RF inductive link efficiency (\( \eta_{\text{RF-Inductive-Link}} \)). For wireless power transmission in air, RF powering is one of the most well-established approaches among common modalities for providing high power density within a constrained specific absorption rate (SAR). Since the maximum geometrical parameters are already set by the application, the main design choice is the operating frequency. Considering the available frequency bands, we chose the 40.68 MHz power carrier frequency band in the industrial-scientific-medical band (ISM-band) as a tradeoff between higher coil quality factors and rectifier switching loss. Lower frequency bands such as the 13.56 MHz band have lower coil quality factors and higher ISM bands such as 433.92 or 915 MHz degrade the PCE for alternating current (AC) to DC conversion at the rectifier due to higher switching loss, which is proportional to frequency [34].

The near-field RF inductive link is designed following the iterative design procedure in [35] with a consideration of existing interconnection to the coils in actual powering system implementation, and its electrical/geometrical parameters
are summarized in Table I. In the high-frequency structural simulator (HFSS) from ANSYS Inc. (Canonsburg, PA, USA), the designed RF inductive link can achieve 86.6% simulated power transmission efficiency (PTE) with no eye rotation and 83.6% PTE with 15° eye rotation, which is likely to be the maximum angle between the transmitter (Tx) coil and Rx coil during the system operation (see Fig. 2). The maximum simulated SAR averaged over 1 g of tissue across the HFSS eyeball model is 0.361 W/kg (see Fig. 3), which is below the FCC regulation, 1.6 W/kg, when the power delivered to the load (PDL) is 186 mW.

### B. Overview of RF-US Relay Chip

The next piece of the system efficiency to maximize is the PCE ($\eta_{\text{PCE}}$) which occurs on the RF-US relay chip as shown in Fig. 1(d). The PCE is made up of the rectifier efficiency ($\eta_{\text{Rect}}$), regulation efficiency ($\eta_{\text{Reg}}$), and the US PA efficiency ($\eta_{\text{US-PA}}$). The chip is roughly divided into the PMU for AC-to-DC power conversion/voltage regulation ($\eta_{\text{Rect}} \times \eta_{\text{Reg}}$) and six-channel PAs ($\eta_{\text{US-PA}}$) for US beamforming. Fig. 4 shows a detailed system diagram including a detailed breakdown of the main circuit blocks of the chip.

Two key designs are used to maximize the PCE. First, the MORR generates and regulates the three supply voltages, needed for programmable amplitude and phase beamforming, including a HV supply in a single step to maximize $\eta_{\text{Rect}} \times \eta_{\text{Reg}}$ while avoiding additional cascaded power loss, as explained in Section III-A. Second, adiabatic low-voltage (LV) PAs, discussed in Section III-C, can improve electrical-to-US PCE by recycling stored charges on parallel capacitors when driving capacitive piezo loads.

To accommodate HVs, class-D HV PAs with an adjustable HV supply allow adjustment of power levels and the flexibility to drive different types of transducers such as piezos,
piezoelectric micromachined ultrasonic transducers (PMUTs),
capacitive micromachined ultrasonic transducers (CMUTs),
and thin-film piezos such as polyvinylidene fluoride (PVDF)
and its composite variants. Overall, the increased efficiency
from the MORR and adiabatic PAs helps reduce the cascaded
power loss and reduces the heating on the relay, allowing for
higher transmit power.

C. US Link and Beamforming

The final piece of the system efficiency is the wireless
power transmission from the relay to the implant $\eta_{\text{US Link}}$ [see
Fig. 1(d)]. US was selected for power transfer between the
relay and implant due to low loss propagation (0.1 dB/cm/MHz
in the vitreous [36], 0.5–1.0 dB/cm/MHz in tissue [21]),
high transduction efficiency, beamforming/focusing capability
[14], [37], and finally a high power safety limit of
7.2 mW/mm² (tissue) and 0.5 mW/mm² (eye) [23]. For exam-
ple, at 1 MHz, the wavelength is around 1.5 mm, which we
can match to the implant Rx for good transducer coupling and
beamforming. Beamforming is critical in implant scenarios
due to the movement of the implant or tissue over time and
variations in implant placement.

For application 1, the retina application [see Fig. 1(a)], the
thickness of the piezo has to be less than the scleral contact
lens thickness, which is typically <1 mm [38]. This means
that we either use the thickness mode at a high frequency
which requires many piezo elements or use a lower frequency
with the area expansion mode [39]. For this proof-of-concept
system, the area expansion mode is used to achieve a large
transmit aperture with a small number of piezo elements.

For a given frequency, the US link is a function of Tx
and Rx aperture sizes [40]. Given our transmit aperture size
(12 mm × 12 mm) and receive aperture (1.5 mm diameter),
the simulated end-to-end US link focusing efficiency ($\eta_{\text{US-link}}$)
using the Field II US simulator at a depth of 2.5 cm [41],
[42] was 2.18%. Compared to [30] which has a US PTE
of 0.66% at 3 cm depth, this link has higher efficiency due
to slightly smaller depth and larger Tx and Rx apertures.
However, unlike [30] that has a fixed focus, the proposed
US link will be programmable to enable dynamic, adaptive
focusing. For comparison, a similar link using midfield RF
powering across 1 cm of air and 4 cm of tissue to a 2-mm
diameter implant achieves 0.04% efficiency [43].

III. CIRCUIT DESIGN AND CONSIDERATIONS

A. MORR and Startup PMU

This section first covers the architecture selection for the
PMU and then the implementation details of the MORR
and startup (SU) PMU.

To maximize $\eta_{\text{Rect}} \times \eta_{\text{Reg}}$ and therefore the system efficiency,
we must carefully select the architecture of the PMU. Fig. 5
shows different possible architectures including conventional
HV-compliance wireless power Rx generating multiple voltage
supplies and our proposed MORR. The conventional structures
shown in Fig. 5(a)–(c) all have limitations either with voltage
tunability, external component count, or cascaded power loss.
The conventional power conversion structure with parallel
rectifiers in Fig. 5(a) has more external capacitors for tuning
the resonant frequency of the secondary coil, and less control
on the absolute rectifier voltage outputs due to the
fixed ratio of the multi-tapped inductor [44]. More common
power conversion structures include a rectifier and DC-to-DC
converters as shown in Fig. 5(b) and (c) [45]. The rectifier
converts the received ac power across an Rx coil into dc power,
and the DC-to-DC converter steps up/down the voltage. This
two-stage power conversion structure imposes cascaded power
losses and results in a lower overall Rx PCE. To improve
the limited PCE, direct resonant current- or voltage-mode
battery charging [46], [47] and reconfigurable resonant reg-
ulating rectifiers [48], [49] were proposed. More recently,
a dual LV output regulating rectifier [50] was proposed for
applications that require different voltage supplies and output
power depending on the operation mode. However, these prior
works are not suitable for IMDs which may require HV,
typically over 10 V, and multiple different supplies. Examples
include neural stimulators, implantable ultrasonic imagers with
CMUTs, and RF-US power relay implants to power neural
probes using beamforming. To address the needs of the above
applications, we designed an HV-compliance MORR and inte-
grated it into the RF-US relay chip.

Next, we will cover the circuit implementation and detailed
operation of the MORR which generates and regulates three
circuit paths for generating each of the supply voltages. The control
of $\text{SW}_{1-3}$ by the switching pulse generator determines which
path the current from the coil flows into. For HV generation,
the HV diode conducts when $V_{\text{IN}}>V_{\text{HV}}$ and converts the
incoming AC voltage into the DC HV ($V_{\text{HV}}<32$ V) when
$\text{SW}_{1}$ is on. As shown in Fig. 6(a), the HV diode consists of
two p-type 36 V laterally diffused metal-oxide semicondu-
citors (LDMOS) for current conduction and a $V_{\text{th}}$ cancellation
circuit to improve the PCE by reducing the voltage drop [51].
The DC HV is controlled by carefully tuning the output power of
the external Tx.

The SU operation is as follows. The HV input bandgap
reference (BGR) and the 4.5/1.8 V HV input linear regulators

![Fig. 5. Conventional structures versus the proposed MORR. (a) Multiple rec-
tifiers with multi-tapped inductor and individual tuning capacitors. (b) Single
low voltage rectifier with step-up and step-down voltage converters. (c) Single
high voltage rectifier with step-down converters. (d) Proposed multi-output
regulating rectifier.](image-url)
start operating with the HV supply that is generated from the HV rectifier. The SU power-on-reset (POR) voltage, $V_{SU\_POR}$, becomes high with $\sim$200 $\mu$s delay after the 1.8 V HV input linear regulator output ($V_{SU\_18}$) becomes stable. Next, the switching pulse generator for the LV regulating rectifiers starts operating with enabled $V_{SU\_POR}$.

For the operation of the two LV paths, the pulse delay modulation (PDM) switching pulse generator controls the half period switching timing to ensure that there is no reverse leakage current through SW1. When SW1 is off, the stored current ($i_{L2}$) in the $L2$-$C2$ tank charges $C_{LV1}$ or $C_{LV2}$. During this phase, $V_{CP}$ instantly changes from 0 to either $V_{LV1}$ or $V_{LV2}$, same as the in-phase current mode of the work with commercial-off-the-shelf (COTS) components in [52]. When $V_{LV1}$ and $V_{LV2}$ reach the target regulating voltages (4.7/2 V), switching pulses are skipped for voltage regulation. Pulse skipping modulation (PSM) was adopted since switching losses for SW1-3 dominate conduction losses for light loads at high switching frequency [34], [53].

Fig. 7 shows the detailed schematic of the switching pulse generator and its key waveforms. A pulse skipping block followed by the zero-crossing detector (ZCD) ($V_{ZCD}$) generates a pulse train ($V_{PS2}$) every $N$ cycles of $V_{ZCD}$ and another pulse train ($V_{PS3}$) one cycle after $V_{PS2}$. As shown in Fig. 7(a), the ZCD circuit consists of five transistors and a buffer stage. Given that the power carrier frequency is 40.68 MHz, the ZCD was designed to have $\sim$300 MHz unity-gain bandwidth and sufficient gain ($\gtrsim40$ dB) at 40.68 MHz. The simulated delay times at the rising and falling edges are 1.3 and 2.4 ns, respectively. The delay induced by the ZCD itself and buffer stages followed by the ZCD can be calibrated by the PDM circuit, which will be explored later in this section. To optimize the switching losses and conduction losses of SW1-3, $N = 4$ was chosen. Two comparators monitor the divided voltages from the regulating rectifier output voltages ($V_{LV1}$ and $V_{LV2}$), which are $V_{SPLS}$ and $V_{SPL2}$. These are generated using 1/4 and 3/5 resistive dividers, respectively. When $V_{SPLS}$ or $V_{SPL2}$ is higher than $V_{HV\_BGR}$, the pulse skipping block skips the pulse of $V_{PS2}$ or $V_{PS3}$ for $V_{LV1}$ or $V_{LV2}$ regulation. $V_{PS2}$, $V_{PS1}$ and their summed pulse, $V_{PS1}$, are fed into separate pulse delay generators so that SW1-3 can be nearly aligned with the positive portion of $i_{L2}$. A finite-state machine (FSM) compares past and present values of $V_{SPLS}$ stored at a voltage sampler and adds or subtracts timing delay with a three-bit up/down counter. When $V_{CP}$ reaches its maximum, outputs of the counter are locked to fix the delay of the switching pulses. The outputs of the pulse trains are level-shifted from 1.8 to 4.5 V and buffered by 4–5 stages with a fan-out of 3, the final stage being $\sim$1/10 of the switch size. SW1 is a transmission gate with a 5 V PMOS with active body biasing (ABB) (8/500 nm) and a 5 V NMOS (8/600 nm). SW2 and SW3 are 5 V MOS devices (4/500 nm) with ABB.

The top left of Fig. 8 shows the schematic of the single-pole dual throw (SPDT) power switch which further reduces power loss by switching to the more efficiently generated $V_{LV1}$ after SU. The right side of Fig. 8 shows the HV regulator implementation for generating $V_{SU\_45/18}$ to ensure stable HV operation. By intentionally lowering $V_{SU\_45}$ 0.2 V below $V_{LV1}$, two integrated Schottky diodes can redirect the power path when $V_{LV1}$ becomes stable. For stable operation across the voltage range (<32 V), $V_{SU\_45/18}$ are designed with stacked 36 V HV LDMOS and 5 V diodes ($D_{1-3}$) to limit $V_{GS}$ for $M_{P6}$, $M_{P7}$, and $M_{P8}$ under 5 V, which is the breakdown voltage for the LDMOS. $M_{N7}$ and $M_{N8}$ improve stability in the light load condition by intentionally pulling current from $V_{SU\_45/18}$. However, when $V_{HV}$ goes higher, the quiescent current of linear regulator becomes larger since $M_{N7}$ and $M_{N8}$

Fig. 6. (a) Operation modes of MORR for the HV, 4.7 and 2 V rectifier output paths and (b) corresponding waveforms.

Fig. 7. (a) Block diagram for PSM and PDM. (b) Circuit topology for ZCD. (c) Waveforms for voltage regulation and maximum power transfer efficiency.

Fig. 8. HV regulator to generate 4.5 and 2 V supplies for the MORR control circuitry during initial SU.
leak more current. To reduce the leakage current at HV, $M_{P9}$ is stacked over $M_{N7}$ and $M_{N8}$ and controlled by $V_{\text{Ctrl}}$. Since $V_{\text{Ctrl}}$ moves along with $V_{HV}$, $V_{GS}$ for $M_{P9}$ becomes smaller and eventually zero when $V_{HV}$ rises.

B. Main PMU

Following the MORR, the main PMU further regulates the output voltages for the analog and digital domains. As shown in Fig. 4, the main PMU consists of a BGR, a 4.5 V low-dropout (LDO) regulator, 1.8 V analog/digital LDOs, a POR, and a negative charge pump (CP). Once $V_{LV1}$ and $V_{LV2}$ generation for the SU PMU is stabilized, the main PMU regulates three voltages (4.5, 1.8 V analog, and 1.8 V digital) to supply cleaner voltages for the four-channel LV PAs since the inherent power supply rejection ratio (PSRR) of the LDOs suppresses the noise on $V_{LV1}$ and $V_{LV2}$. The post-layout simulated values of PSRR for 4.5 and 1.8 V LDOs are $-28.8$ and $-40.5$ dB within DC-to-1 kHz bandwidth both with 0.2 V dropout voltage and with 2 mA and 500 $\mu$A current loads, respectively. The negative CP sets the HV ground 5 V lower than $V_{HV}$ for the level-shifted PMOS gate drivers to avoid the gate oxide breakdown of the HV devices in the HV PAs. The POR provides an enable signal to the digital circuits for the PAs.

C. Ultrasound PAs

US PAs are designed to maximize $\eta_{\text{US-PA}}$ and therefore the overall system efficiency while maintaining the flexibility to drive multiple types of transducers including piezoe, PMUTs, CMUTs, and thin-film piezos for different applications. To achieve this, the PA should be able to operate from 100s of kHz to 10 MHz depending on the transducer and resonant mode selected. Two types of US PAs were designed for this chip: adiabatic PAs which maximized the efficiency for nominal operation and HV PAs to accommodate implants that require higher power or are placed deeper in the body.

HV PAs were implemented using HV 29 V LDMOS devices operating in class-D mode as shown in Fig. 4. HV allows the transmitted power to be adjusted and can also be used to drive high-impedance transducers. The piezo acts as a filter to remove the high-frequency components, so no additional filtering is needed. Since LDMOS devices can only handle a small $V_{gs}$, we used HV level shifters [54] to allow operation across a wide voltage range (6–29 V) for driving frequencies up to 10 MHz.

For the LV PAs, we increased the efficiency of driving capacitive piezoelectric loads by implementing adiabatic PAs. When driving a capacitive load, the energy stored on the capacitance is dissipated through the switches on each cycle and decreases the PCE of the PA. One way to alleviate this problem is to use an inductor to resonate out the capacitance, but at MHz frequency and pF capacitance, this results in large inductors in the mH or $\mu$H range, which is too bulky to implement on-chip.

The same problem is faced in digital circuits for clock drivers with large capacitive loads, which can be solved using adiabatic charging [55], [56]. The voltage recovered can be boosted by increasing the individual capacitor size and the number of parallel capacitors.

The basic operation of the differential adiabatic PA is as follows. First, the load is charged to the supply voltage. Next the parallel capacitors are connected one at a time to extract charge from the load; in steady state, the voltage on each of the parallel capacitors is an intermediate voltage between the supply voltage and ground, so that connecting the capacitors to the load will create the downward blue staircase pattern (see Fig. 9). Once the final capacitor is disconnected, the load is shorted, and the capacitors are then reconnected to the load in the opposite polarity one at a time in reverse order to charge it using the energy stored on the parallel capacitors forming the red upward staircase pattern. The recycling of charge by the parallel capacitors will restore the voltage to $V_{flip}$ at which point the supply voltage charges the load to replenish the lost energy. This cycle describes the first half period; the cycle is repeated for the opposite polarity to complete one period of the driving waveform. The detailed derivation of the adiabatic efficiency is described in Appendix A. The ratio of the voltage after charge recycling is

$$\frac{V_{flip}}{V_{DD}} = \frac{n \pi}{1 + (n + 1)x}$$

where $n$ is the number of parallel capacitors and $x = C_f/C_P$, the ratio of the parallel capacitor ($C_f$) to the load capacitor ($C_P$). The efficiency of the adiabatic PA neglecting control circuitry is given by

$$\eta = \frac{4\beta^2 \sin(1 - a)^2}{\pi^2 RC_P f \left(1 - \frac{V_{lip}}{V_{in}}\right)^2 + 4\beta^2 \sin(1 - a)^2}$$

$$\beta = \frac{V_R}{V_{\text{Piezo}}} = \sqrt{\frac{R}{R^2 + \left(2\pi f L_S - \frac{1}{2\pi C_f}\right)^2}}$$

$$\alpha \equiv 1 - \frac{t_{\text{rise}}}{t_{\text{period}}}.$$
$n$ is increased. The efficiency equation is plotted with $a$ in Fig. 10(b) for a different number of parallel flipping capacitors ($n$) for the typically extracted impedance model parameters at 850 kHz. As a comparison, the efficiency for class-D mode is shown as well. From our model, we expect about a 37% increase in efficiency with adiabatic mode compared to a class-D mode for our implementation.

The circuit implementation is shown in Fig. 9. The circuit uses a delay-locked loop (DLL) to generate the short pulses to save power compared to using a clock eight times faster. The input clock at four times the center frequency increments to save power compared to using a clock eight times faster. The DLL pulses and $S[0], \ldots, S[3]$ are inputs to a DLL that generates eight pulses per $S[1]$ and $S[3]$. The output DLL waveforms for $S[0], \ldots, S[3]$ are then put through a lookup table (LUT) to generate the control waveforms $\Phi_1, \ldots, \Phi_{14}$. The delay cells of the DLL were implemented using a current starved inverter chain and a five-bit thermometer current DAC incremented or decremented the current reference for the delay cells after looking at the eighth and ninth delay.

To implement beamforming, the phase of $S[0], \ldots, S[3]$ for each channel can be modified by adding a two-bit phase code to the accumulator. $S[1]$ and $S[3]$ are inputs to a DLL that generates eight pulses per $S[1]$ and $S[3]$. The output DLL waveforms for $S[0], \ldots, S[3]$ are then put through a lookup table (LUT) to generate the control waveforms $\Phi_1, \ldots, \Phi_{14}$. The delay cells of the DLL were implemented using a current starved inverter chain and a five-bit thermometer current DAC incremented or decremented the current reference for the delay cells after looking at the eighth and ninth delay.

The simulated adiabatic PA efficiency to the real part of the load was 75.6% for the load values shown in Fig. 10, with an expected 66.5% efficiency to the radiation resistance for a dielectric loss resistance of 50 $\Omega$. Compared to the simulated class-D mode efficiency, adiabatic mode had an improvement of 33.3%. This is a little lower than the model as expected since signal generation and switch drivers were not taken into account.

### IV. Measurements

#### A. Multi-Output Regulating Rectifier

To verify the operation of the MORR, we measured key waveforms from the chip (see Fig. 11 for the die photograph). Fig. 12 shows measured transient waveforms during the MORR SU with the SPDT power switch operation. All SU circuits ($V_{HV\_BGR}$, $V_{SU\_45}$, and $V_{SU\_POR}$) power up within 240 $\mu$s, while the load capacitor ($C_{HV} = 1 \mu F$) charges up to 32 $V$. Afterward, $V_{LV1}$ and $V_{LV2}$ start charging up by PDM and PSM switching operation with enabled $V_{SU\_POR}$. With stabilized $V_{LV1}$, the SPDT starts drawing more power from $V_{LV1}$ since $V_{LV1} > V_{SU\_45} + 0.2$ $V$ as shown in Fig. 12. The SPDT improves the PCE by $\sim 3\%$ (simulation) at 186 mW load ($P_L$), and this PCE improvement can be indirectly observed by the $V_{HV}$ increase during the switch transition (see Fig. 12). Fig. 13(a) shows the operation of the PDM. The current value for 1/4 of $V_{LV1}$ is compared to its past value every two cycles of a 312.5 kHz reference clock divided from $f_0$. The counter adjusts the timing of $SW_{i-3}$ up or down so that $V_{LV1}$ increases. When $V_{LV1}$ approaches $\sim 4.5$, 0.2 $V$ lower than the target regulating voltage, the PDM counter becomes locked in order to avoid an oscillation due to counting up and down and the PSM continues to regulate $V_{LV1}$ to the target regulating voltage.

![Fig. 10](image1.png)  
(a) Typical piezo impedance of a PA channel and piezo circuit model. (b) Efficiency for ideal adiabatic PA for a different number of flipping capacitors ($n$) and waveform rise times. Piezo model parameters for a typical PA channel are shown. (c) Photograph of the piezo array. (d) Beamforming simulation of 12-element piezo array.

![Fig. 11](image2.png)  
Fig. 11. Die micrograph of the proposed RF-US relay chip.

![Fig. 12](image3.png)  
(a) SU waveforms for the HV rectifier and HV regulators. (b) Power switch switching from $V_{LV1}$ to $V_{SU\_45}$ resulting in increased conversion efficiency of the MORR.
Fig. 13. (a) Measurement of improved alignment of the switching pulse with the inductor current once the PDM loop stabilizes (UP goes low and the three-bit counter locks). The zoomed-in waveforms show a higher voltage at the rectifier input \( V_{CP} \) after alignment. (b) PSM for the 4.7 and 2 V output waveforms are shown.

Voltage of 4.7 V. Fig. 13(b) shows the key waveforms for voltage regulation by PSM. When \( V_{LV1} \) or \( V_{LV2} \) goes below the target regulating voltage, \( C_{LV1} \) or \( C_{LV2} \) is charged through closed \( SW_2 \) or \( SW_3 \), respectively. The loop response of PSM is \( \sim 10 \times \) faster than the one of PDM to avoid a conflict between two loop responses. The measured line regulations for \( V_{LV1} \) and \( V_{LV2} \) are 1.4% and 0.6% when \( V_{HV} = 5\sim10 \) V. The load regulation of \( V_{LV1} \) and \( V_{LV2} \) are 10.9 and 25 mV/mA when the loads change from 0 to their maximums, which are 10 and 2 mA, respectively. The measured PCE at the target load power, 186 mW, is 81%. The PTE of the fabricated inductive link at \( f_0 = 40.68 \) MHz is 85.5% when \( R_L = 537 \) \( \Omega \) corresponding to 186 mW at \( V_{HV} = 10 \) V [see Fig. 14(d)].

B. US PA and US Link

To verify the operation of the US PAs, they were characterized together with the US link. The power supplies used for the US PAs (6–29, 4.5, and 1.8 V) were supplied using a DC power supply to measure the consumed power. The chip used four 4.5-V adiabatic channels and two HV channels to drive the piezo array at 850 kHz consisting of 12 \( 2 \) mm \( \times \) 2 mm \( \times \) 0.4 mm piezo elements spaced 1 mm apart, with each channel driving two adjacent elements to increase the aperture size given the limited number of channels. In this configuration, there is a negligible loss in focusing efficiency when the US Rx is centered over the array compared to a phased array with arbitrary phase control over each element and increasing loss as the Rx is moved outwards.

In Field II simulations, at a 3.5 mm offset in both the \( x \) and \( y \) directions, the focusing efficiency is about half of an ideal phased array. To potentially fit the array on a scleral lens (<1 mm thick) for the retina application, we utilize the area expansion mode to decrease the thickness. The piezo array was submerged in mineral oil to mimic tissue loss, and the acoustic power was measured using a 1.5-mm diameter needle hydrophone (ONDA HNC 1500). The PA + US link efficiency was calculated using \( \eta_{US-PA} \times \eta_{US-Link} = \frac{P_{RX}}{P_{dc,chip}} \).

Performance was first characterized from 2.5 to 5 cm depths (\( Z \)-direction) for the adiabatic mode, class-D mode, and beamforming mode as shown in Fig. 14(a). The adiabatic mode shows a 30%–40% increase in efficiency compared to class-D mode, which is in line with our calculation prediction of 37% and our simulation of 33.3%. The efficiency range and variation with distance are due to variation in piezo impedances within the array, which influences the improvement of adiabatic mode over class-D mode per channel. Depending on the beamforming code, different channels will contribute more or less to the final array efficiency. Beamforming mode compared to unfocused mode has higher efficiency across the whole range with about the same efficiency at the natural focus of the array (3 cm) and a 251% improvement near the retinal application distance of 2.5 cm. Next, we characterized the tradeoff of adjusting the HV supply in Fig. 14(b) by sweeping the HV supply and measuring the PA + US link efficiency as well as the available power at the hydrophone. As expected, increasing the HV supply allows us to increase the received acoustic power but decreases the efficiency because the power becomes dominated by the two HV channels, leaving most of the aperture unused.
TABLE II

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<td>2 Coil</td>
<td>4 Coil</td>
<td>Magnetostrict</td>
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<td>Miodid (RF)</td>
<td>US</td>
<td>2 Coil + US</td>
<td>2 Coil + US</td>
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<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<td>Consider ac</td>
<td>Yes</td>
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<td>Yes</td>
<td>Yes</td>
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<td>tissue interface loss</td>
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<td>Distance (mm) (medium)</td>
<td>12</td>
<td>70</td>
<td>0.50</td>
<td>3</td>
<td>10</td>
<td>40</td>
<td>30</td>
<td>12</td>
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<tr>
<td></td>
<td>(Lamb rib)</td>
<td>(Air)</td>
<td>(Saline)</td>
<td>(Air / Luid beam phantom)</td>
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<tr>
<td>Ex-Vivo Measurement</td>
<td>RF through rib</td>
<td>6 Viva neural probe (emb)</td>
<td>-</td>
<td>-</td>
<td>Precise chest</td>
<td>-</td>
<td>-</td>
<td>US through pig eye</td>
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<td>PDL (mw)</td>
<td>-</td>
<td>35</td>
<td>0.39</td>
<td>0.16</td>
<td>&lt;0.00013</td>
<td>(Air)</td>
<td>0.195</td>
<td>0.0288</td>
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<tr>
<td>External transmitter aperture</td>
<td>17.22 mm diameter</td>
<td>13 cm diameter</td>
<td>25 mm diameter</td>
<td>2 x 2 mm²</td>
<td>6 x 6 mm²</td>
<td>25.4 mm diameter</td>
<td>Relay Rx coil 15 x 17 mm²</td>
<td>External 32 mm diameter</td>
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<tr>
<td>Implant receiver aperture</td>
<td>4 x 4 mm²</td>
<td>19 x 19 mm³</td>
<td>4 x 2 mm²</td>
<td>0.5 x 0.5 mm³</td>
<td>2 mm diameter</td>
<td>0.54 mm³</td>
<td>1.1 mm diameter</td>
<td>1.3 mm diameter</td>
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|                           |       |       |       |       |       |       |       |       |
| D/avg Rx With             | <10   |     |     | >10   |     |     |     |     |
|                           |     |     |     |     |     |     |     |     |
| Efficiency (%)            | PTE 3.05 | PTE 20.5 | PTE 0.08-0.008 | - | PTE 0.04 | RF Inductive Link 25 | US Link 0.66 | Total end-to-end system efficiency: 0.27² |

|                           |       |       |       |       |       |       |       |       |
|                           |       |       |       |       |       |       |       |       |

* Total end-to-end efficiency from DC power of the PA on the glasses to Rx acoustic power
1 Measured when $V_{HV} = 10 \text{ V}$
2 DC supply power of the US PA to acoustic power at the hydrophone

XY plane beamforming was tested across 16 points from −6 to 6 mm from the center of the array. In Fig. 14(c) for fixed focusing, power was focused to 25 mm away centered over the array $(x, y, z) = (0, 0, 25 \text{ mm})$ where the origin is the center of the piezo array. Then, the hydrophone was moved across the XY plane without adjusting the focus. For beamforming mode (focused), the focus was changed for each point for maximum efficiency. Compared to the fixed focus case which only has high efficiency for a single point, focusing on each point can maintain close to maximum efficiency of around 1.5% across a 4 mm range.

C. End-to-End Wireless Test

The RF-US relay system is demonstrated through an in vitro full wireless test as shown in Fig. 15 which includes the RF PA, RF inductive link, the relay chip, and US link. An external class-E RF PA drives the Tx coil on the glasses at 40.68 MHz and transmits power to the Rx coil 1.2 cm away in the air. The Rx coil receives the incoming AC power and powers up the relay chip. The relay chip converts the AC power to DC power to operate the six-channel PAs driving the piezo array submerged in mineral oil at 850 kHz. The transmitted passes through an agar eyeball phantom to the hydrophone 29 mm away. The reported end-to-end efficiency is defined as the received acoustic power at the hydrophone divided by the power drawn from the DC power supply for the RF PA. The efficiency breakdown is shown in Table II.

Finally, we also verified the US PA + US link efficiency through a fresh pig eyeball with the piezo array 26.2 mm away from the hydrophone [see Fig. 15 (top left)] reaching a peak acoustic received power of 0.794 mW and efficiency of 0.83%. This efficiency, which includes the PA and US link efficiency, is comparable to that of the US link in [30] which has a similar separation distance. Compared to a pure RF solution [43] which has a similar separation distance and Rx size, the end-to-end system efficiency of this work is about seven times higher. The efficiency is slightly lower in the pig eyeball compared to mineral oil due to the differences in the speed of sound of tissue within the eye which causes additional reflections, but we expect the efficiency to be higher in the actual implant scenario when the epiretinal implant sits on the surface of the retina; the US will not need to travel through the retina, choroid, and sclera at the back of the eye.

V. Conclusion

We have demonstrated the first RF-relay with beamforming for powering mm-sized IMDs. To increase the system efficiency, the cascaded power loss from the multi-modality relay approach was ameliorated with our rectifier and PA designs.
The MORR generates three voltage supplies in a single step to remove extra cascaded power loss terms. The adiabatic PA re-uses energy from the capacitive part of the piezo load to increase the driving efficiency.

To understand the comparison between the various state-of-the-art implant wireless powering works in Table II, it is useful to look at the distance to average Rx width ratio, as this helps determine if we are in the strong coupling or weak coupling regime. We expect in the strong coupling regime that inductive links become very efficient as demonstrated by [18] and [19]. In the weak coupling regime when the distance to Rx ratio becomes large, US links become preferred and can achieve moderate efficiencies from 0.1% to 1% and PDL up to around 1 mW.

This work is the first to demonstrate US beamforming capability for powering implants with an RF-US relay. Compared to [29], this work addresses the loss at the media interface, and compared to [30], this work integrates the power conversion from RF to DC to US in a chip to incorporate flexibility with similar transducer sizes. To the best of our knowledge, this work has the highest PDL while maintaining a higher overall efficiency for links with similar Rx dimensions and implant depth.

APPENDIX A
ADIABATIC EFFICIENCY DERIVATION

To the best of the author’s knowledge, this is the first derivation for the power efficiency of driving a piezoelectric transducer load with an adiabatic PA. The derivation of the upper bound efficiency of the adiabatic PA neglects the power needed to generate control signals and assumes ideal switches.

A. Voltage Efficiency

This section will cover the derivation for the ratio of the voltage recovered from adiabatic charging. A typical circuit model for a piezo is shown in Fig. 10(a). To simplify the analysis we will only consider the parallel capacitance ($C_p$) of the load during the adiabatic charging parts, which allows us to use charge balance equations to find the restored voltage. This is a good approximation since charge sharing between parallel capacitors in the PA happens at frequencies much higher than the fundamental frequency, so the inductor $L_s$ will make the series RLC path high impedance compared to $C_p$.

We will denote $V_1, \ldots, V_n$ to be the steady-state voltages on the parallel flipping capacitors $C_1, \ldots, C_n$ and define

$$x_i = \frac{C_i}{C_p}. \quad (7)$$

where $V_{d(i)}$ denotes the voltage across the capacitor $C_i$ after discharge phase $i$. Starting from when the load is fully charged, we write the charge balance equations during the discharge phase as each capacitor $C_i$ is connected to the load one at a time to extract charge

$$V_{dd} + V_{1,i}x_1 = V_{d1}(1 + x_1) \quad (8)$$
$$V_{d1} + V_{2,i}x_2 = V_{d2}(1 + x_2) \quad (9)$$
$$\ldots \quad (10)$$
$$V_{d(n-1)} + V_{n,i}x_n = V_{dn}(1 + x_n). \quad (11)$$

Once discharge is finished, the voltage across the load is shorted before capacitors are reconnected in reverse order one at a time to recharge the load in the opposite polarity. We can then write the charge balance equations for the charging phase

$$V_d n x_n = V_n(1 + x_n) \quad (12)$$
$$V_n + V_{d(n-1)}x_{n-1} = V_{n-1}(1 + x_{n-1}) \quad (13)$$
$$\ldots \quad (14)$$
$$V_2 + V_d 1 x_1 = V_1(1 + x_1). \quad (15)$$

Since we are interested in the steady state, we can equate $V_i$ of the discharging phase to the $V_i$ of the charging phase. Using the above set of equations we can solve for $V_1$, the voltage on the load capacitor after the charging phase, which is exactly the restored voltage from adiabatic charging $V_{flip}$

$$V_1 = V_{flip} = V_{dd} \left( \frac{n \times}{1 + (n + 1) \times} \right) \quad (16)$$
$$\frac{V_{flip}}{V_{dd}} = \frac{n \times}{1 + (n + 1) \times}. \quad (17)$$

Note that $x_1, \ldots, x_n$ all contribute the same to the output, so in order to maximize the voltage on the load capacitor we set $x_1, \ldots, x_n = x$.

B. Adiabatic Power Efficiency

Now that we know $V_{flip}$, we will now derive how this translates to power efficiency. To simplify the analysis, we will assume that there is a sufficient number of parallel capacitors such that the waveform approximates a trapezoidal waveform with rising time $t_{rise}$, period $t_{period}$, and pulselwidth $\tau$.

The amplitude of the fundamental frequency of a trapezoidal waveform by using the Fourier series is

$$V_{fund} = 4V_{dd} \frac{t_{rise}}{t_{period}} \sin \left( \frac{\tau}{t_{period}} \right) \sin \left( \frac{t_{rise}}{t_{period}} \right) \quad (18)$$
$$V_{fund} = V_{dd} \left( \frac{4 \pi}{\tau_{rise}} \right) \sin \left( \frac{t_{rise}}{t_{period}} \right) \quad (19)$$

where the wave swings from $V_{dd}$ to $-V_{dd}$. The above simplification comes from the fact that the pulselwidth is always half of the period for a symmetric waveform. Since we have recovered some of the voltage from the adiabatic PA scheme, the power used to recharge the capacitor per cycle from $V_1$ to $V_{dd}$ is

$$P_c = 2C_p (\Delta V)^2 f \quad (20)$$
$$P_c = 2C_p (V_{dd} - V_1)^2 \frac{1}{t_{period}} \quad (21)$$

The factor of 2 is from having to charge the capacitor twice per cycle, one for each of the negative and positive polarities of the differential waveform.

To calculate the PDL we first find the voltage division ratio from the series inductor and capacitor impedance

$$\beta = \frac{V_{R}}{V_{piezo}} = \frac{R}{\sqrt{R^2 + (2\pi f L_s - \frac{1}{2\pi f c})^2}} \quad (23)$$
The PDL at the center frequency is

\[
\eta = \frac{(\beta V_{DD}(\frac{\pi}{2}))\text{csc}(\frac{\text{rise}}{\text{period}})^2}{4R} \text{sinc}(x) \approx \frac{\sin(\pi x)}{\pi x}.
\]

Therefore, the power efficiency is the PDL divided by the sum of the PDL and the power used to recharge the capacitor

\[
\eta = \frac{2CP(V_{DD} - V_{1})f + \frac{(\beta V_{DD}(\frac{\pi}{2}))\text{csc}(\frac{\text{rise}}{\text{period}})^2}{4R}}{\pi^2RC_P f(1 - \frac{V_{in}}{V_{DD}})^2 + 4\beta^2\text{sinc}(1-\alpha)^2
\]

\[
a \equiv 1 - \frac{t_{\text{rise}}}{t_{\text{period}}}
\]

\[\text{(28)}\]

C. Comparison With Class-D

To compare with the adiabatic operation, class-D efficiency was also derived. We follow a similar derivation. The power at the fundamental frequency for a square wave is

\[
V_{\text{fund},D} = V_{DD} \left(\frac{4}{\pi}\right)
\]

and the power to charge the capacitor per cycle is

\[
P_{C,D} = C_P (\Delta V)^2 f
\]

\[\text{(30)}\]

Unlike the adiabatic case, the charging only happens once per period and is done in a single step, so \(\Delta V = 2V_{DD}\).

The power efficiency of the class-D mode is

\[
\eta_D = \frac{(\beta V_{DD}(\frac{\pi}{2}))\text{csc}(\frac{\text{rise}}{\text{period}})^2}{4R} \frac{4C_P V_{DD} f + (\beta V_{DD}(\frac{\pi}{2}))\text{csc}(\frac{\text{rise}}{\text{period}})^2}{4R}
\]

\[\text{(32)}\]

\[\text{(33)}\]

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REFERENCES


Ernest So (Graduate Student Member, IEEE) received the B.S. and M.S.E. degrees in biomedical engineering from Johns Hopkins University, Baltimore, MD, USA, in 2014 and 2016, respectively, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2018, where he is currently pursuing the Ph.D. degree in electrical engineering.

From 2014 to 2016, he worked with Professor Nitish Thakor at Johns Hopkins University designing neural recording circuits and low-noise CMOS image sensors for medical imaging. His current thesis work with Professor Amin Arbabian at Stanford University involves wireless power and data communication for implantable devices.

Mr. So was a recipient of the Stanford Graduate Fellowship in 2016 and the IEEE Solid-State Circuit Society (SSCS)-Brain Best Paper Award in 2021.
Pyungwoo Yeon (Member, IEEE) received the B.S. degree in electrical and computer engineering from Seoul National University, Seoul, South Korea, in 2010, the M.S. degree in electrical engineering and information systems from The University of Tokyo, Tokyo, Japan, in 2012, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2019.

From 2012 to 2014, he was with the Power Management IC Team, Samsung Electronics, Yongin, South Korea, where he contributed to prototyping an Alliance for Wireless Power (A4WP) (currently AirFuel)-compatible wireless charger IC. He spent the first quarter of 2019 with the Display EE Team, Apple Inc., Cupertino, CA, USA. In September 2019, he joined Stanford University, Stanford, CA, USA, as a Post-Doctoral Fellow in electrical engineering. Since 2021, he has been a Sensor Design Engineer with Apple Inc. His research interests include novel system architectures and circuit topologies for wireless implantable, wearable, and IoT medical therapeutics/diagnostics.

Dr. Yeon was a co-recipient of the IEEE Wireless Power Transfer Conference (WPTC) Best Paper Award in 2013, the Silver Award in the Samsung Electro-Mechanics Best Paper in 2016, the Third IEEE Biomedical Circuits and Systems Conference (BioCAS) Best Paper Award in 2017, the Stanford Respond Innovate Scale Empower (RISE) SARS-CoV-2 (COVID-19) Crisis Response Trainee Seed Grant Program Award in 2020, and the IEEE Solid-State Circuit Society (SSCS)-Brain Best Paper Award in 2021.

E. J. Chichilnisky (Member, IEEE) received the B.A. degree in mathematics from Princeton University, Princeton, NJ, USA, in 1985, and the M.S. degree in mathematics and the Ph.D. degree in neuroscience from Stanford University, Stanford, CA, USA, in 1992 and 1995, respectively.

He is currently the John R. Adler Professor of neurosurgery and a Professor of ophthalmology with neurosciences at Stanford University, where he has been working since 2013. Previously, he worked with the Salk Institute for Biological Studies, La Jolla, CA, USA, for 15 years. His research has focused on understanding the spatiotemporal patterns of electrical activity in the retina that convey visual information to the brain, and their origins in retinal circuitry, using large-scale multi-electrode recordings. His ongoing work now focuses on using basic science knowledge along with electrical stimulation to develop a novel high-fidelity artificial retina for treating incurable blindness.

Dr. Chichilnisky was a recipient of the Alfred P. Sloan Research Fellowship, the McKnight Scholar Award, the McKnight Technological Innovation in Neuroscience Award, and the Research to Prevent Blindness Stein Innovation Award.

Amin Arbabian (Senior Member, IEEE) received the Ph.D. degree in electrical engineering and computer science from the University of California at Berkeley, Berkeley, CA, USA, in 2011.

From 2007 to 2008, he was a part of the Initial Engineering Team, Tagarray, Inc., Palo Alto, CA, USA (now acquired by Maxim Integrated Inc., San Jose, CA, USA). In 2010, he joined Qualcomm’s Corporate Research and Development Division, San Diego, CA, USA, where he designed circuits for next-generation ultralow power wireless transceivers. In 2012, he joined Stanford University, Stanford, CA, USA, where he is currently an Associate Professor of electrical engineering. His current research interests include mm-wave and high-frequency circuits and systems, imaging technologies, the Internet-of-Everything devices (including wireless power delivery techniques), and medical implants.

Dr. Arbabian was a recipient or a co-recipient of the 2020 IEEE Transactions on Biomedical Circuits and Systems Best Paper Award; the 2016 Stanford University Tau Beta Pi Award for Excellence in Undergraduate Teaching; the 2015 NSF Faculty Early Career Development Program (CAREER) Award; the 2014 Defense Advanced Research Projects Agency (DARPA) Young Faculty Award (including the Director’s Fellowship in 2016); the 2013 Hellman Faculty Scholarship; the 2010–2011, 2014–2015, and 2016–2017 Qualcomm Innovation Fellowships; and best paper awards at the 2017 IEEE Biomedical Circuits and Systems Conference; the 2016 IEEE Conference on Biomedical Wireless Technologies, Networks, and Sensing Systems; the 2014 IEEE VLSI Symposium; the 2013 IEEE International Conference on Ultra-Wideband; the 2010 IEEE Jack Kilby Award for Outstanding Student Paper at the International Solid State Circuits Conference; and two-time second place best student paper awards at 2008 and 2011 Radio Frequency Integrated Circuits (RFIC) Symposiums. He currently serves on the steering committee for the RFIC Symposium, the technical program committees of the RFIC Symposium and the VLSI Symposium, and as an Associate Editor for IEEE Solid-State Circuits Letters and the IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology.