# A 1024-Channel 268-nW/Pixel 36 × 36 $\mu$m$^2$/Channel Data-Compressive Neural Recording IC for High-Bandwidth Brain–Computer Interfaces

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***Abstract*— This article presents a data-compressive neural recording IC for single-cell resolution high-bandwidth brain–computer interfaces (BCIs). The IC features wired-OR lossy compression during digitization, thus preventing data deluge and massive data movement. By discarding unwanted baseline samples of the neural signals, the output data rate is reduced by 146× on average while allowing the reconstruction of spike samples. The recording array consists of pulse-position modulation (PPM)-based active digital pixels (ADPs) with a global single-slope (SS) analog-to-digital conversion scheme, which enables a low-power and compact pixel design with significantly simple routing and low array readout energy. Fabricated in a 28-nm CMOS process, the neural recording IC features 1024 channels (i.e., 32 × 32 array) with a pixel pitch of 36 $\mu$m that can be directly matched to a high-density micro-electrode array (MEA). The pixel achieves 7.4-$\mu$V$_{\text{rms}}$ input-referred noise with a −3-dB bandwidth of 300 Hz–5 kHz while consuming only 268 nW from a single 1-V supply. The IC achieves the smallest area per channel (36 × 36 $\mu$m$^2$) and the highest energy efficiency among the state-of-the-art neural recording ICs published to date.**

***Index Terms*— Brain–computer interface (BCI), brain–machine interface (BMI), compression, multi-electrode array, neural interface, neural recording, pulse-position modulation (PPM), single-cell resolution.**

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## I. Introduction

BRAIN–COMPUTER interfaces (BCIs) have the potential to revolutionize therapy for neurological diseases, because they target the nervous system with high spatiotemporal resolution as opposed to pharmacological, surgical, or gene therapies [1], [2], [3]. Next-generation BCIs for clinical applications will benefit from an implantable neural recording IC with a dense, high channel count recording array that can be directly matched to a micro-electrode array (MEA) at the pitch of neurons (≈30 $\mu$m) to effectively capture spatiotemporal patterns of neural activity at single-cell resolution. Over the last five decades, the doubling rate for simultaneously recorded neurons was approximately seven years, and the number is still less than a few thousand [4]. Future BCIs must support simultaneous recording from tens of thousands of neurons or more within the form factor and power budget of a fully implanted device. Recently, custom requirements for clinical BCIs that focus only on action potentials are emerging [5], [6], [7]. Hence, there is an opportunity for an architectural paradigm shift that can increase the number of

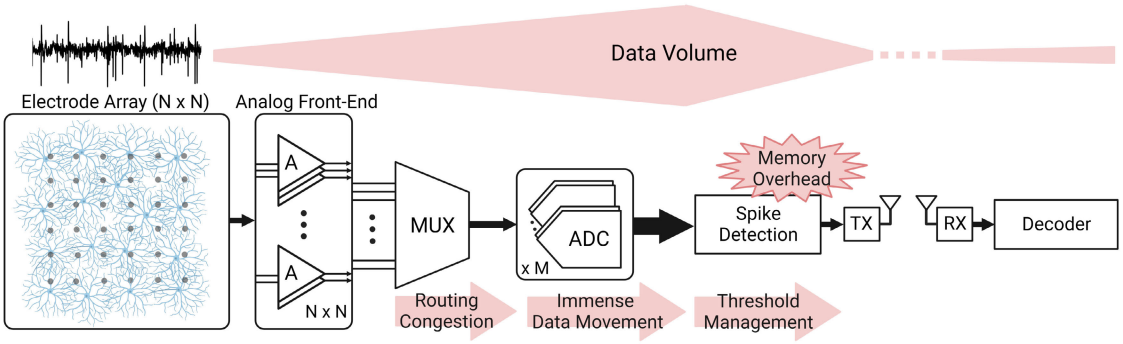


Fig. 1. Design challenges of neural recording ICs for massive MEA and issues of the prior works.

channels while reducing channel area and power consumption. However, meeting these requirements poses a number of significant design challenges [8] (see Fig. 1). First, as the number of channels ($N^2$) increases, the system data rate becomes unmanageable (e.g., 10 000 channels digitized at 10-bit resolution and 20 kS/s generate 2 Gb/s). On-chip spike detection (SD) can compress the raw data by transmitting only a snippet around the spike [9], [10]. However, this solution incurs significant overhead in threshold management, typically per channel, and in the memory, buffers needed to compensate for the SD latency. Compressive sensing [11], [12] and compressive autoencoder [13] architectures can be designed with hardware-friendly encoders on the implant site. However, they require all raw data to be digitized and buffered. Notably, the data movement cost can be a limiting factor when compression happens after digitization (e.g., to buffer 1-ms spikes in the above case, caching 2 Mbit into a 0.6-pJ/bit SRAM [14] at 1 kHz consumes 1.2 mW). Analog implementations of compressive sensing reduce the amount of raw data that are digitized [11], but require bulky analog filters that do not scale well to large-scale high-density arrays. Second, as the channel density increases, the routing from the analog signals in the array to the peripheral recording channels becomes a limiting factor. A common strategy is to perform sub-array digitization using a switch matrix [15], [16]. However, this eliminates the possibility of simultaneous recording over the entire array. Active digital pixels (ADPs) digitize the analog input inside the array and reduce routing congestion [17], but it comes at the cost of large pixels. Third, most of the prior high-density neural recording ICs consume chip total power per channel of more than 10 $\mu$W. Practical wirelessly powered biomedical implants have a power budget of less than 10 mW [18]. Hence, the number of channels ($N^2$) is limited to less than 1000. Also, as the size of the channel is getting smaller, power density increases, and it leads to a safety issue along with a maximum allowable heat dissipation of implantable device in direct contact with a tissue (e.g., a power dissipation limit of 1 mW/mm$^2$ requires less than 1 $\mu$W per channel in the area of 33 $\times$ 33 $\mu$m). Finally, for all the prior works, the area of the channel is too large (>0.004 mm$^2$) to achieve a single-cell resolution neural interface in most regions of the nervous system.

This article presents a data-compressive neural recording IC that addresses the above issues to realize a high-density and channel count recording array for future single-cell resolution BCIs. The 1024-channel array consists of in-pixel pulse-position modulation (PPM)-based ADPs with a global single-slope (SS) A/D conversion scheme that significantly reduces the design complexity and size of the pixel. Different from [19] employing only a global SS A/D conversion to reduce the size of digital pixel, the PPM-based ADP output is read outside the array with a single routing line, thus significantly reducing the array's routing congestion and readout energy. A wired-OR compression method [20] compresses massive data from the large array during the A/D conversion, which addresses the data deluge problem and significantly reduces data movement. The average compression rate is 146$\times$ with pre-recorded neural signals, while the reconstructed signal enables efficient spike sorting, cell type classification, and recovery of cell mosaics [20], [21]. Since the compression occurs without a spike detector, there is no threshold management and memory overhead. Fabricated in a 28-nm CMOS process, it achieves the lowest power consumption per channel (=268 nW) and the smallest area per channel (=36 $\times$ 36 $\mu$m$^2$) among neural recording ICs while having 7.4-$\mu$V$_{\text{rms}}$ input-referred noise in a [0.3, 5]-kHz bandwidth.

As an extension of [22], this article is organized as follows. Section II presents a system overview of the neural recording IC, while its architectural benefits are described in Section III. Section IV provides implementation details, and the measurement results are presented in Section V. Finally, the conclusions are drawn in Section VI.

## II. System Overview

### A. Neural Recording IC Architecture Overview

Fig. 2 shows the block diagram of the data-compressive neural recording IC. At the front end, the $N \times N$ MEA interfaces with the neural cells, and the pitch-matched ADP directly reads out each electrode in the $N \times N$ pixel array. Each ADP consists of a front-end amplifier, comparator, and wired-OR logic. Outside the array, the global ramp generator, counter, and collision decoder process the array output data.

First, the input from the electrode is conditioned by the amplifier in the band of interest. The continuous-time (CT) comparator in the pixel applies PPM to the output of the amplifier using a globally distributed ramp signal. Then, the PPM output is connected to the row and column address of each pixel through wired-OR logic. In this way, the

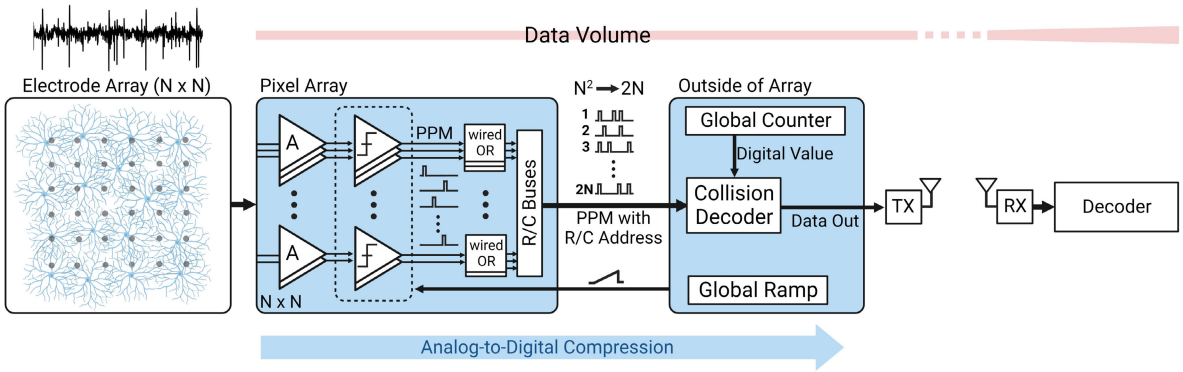


Fig. 2. Block diagram of the data-compressive neural recording IC.

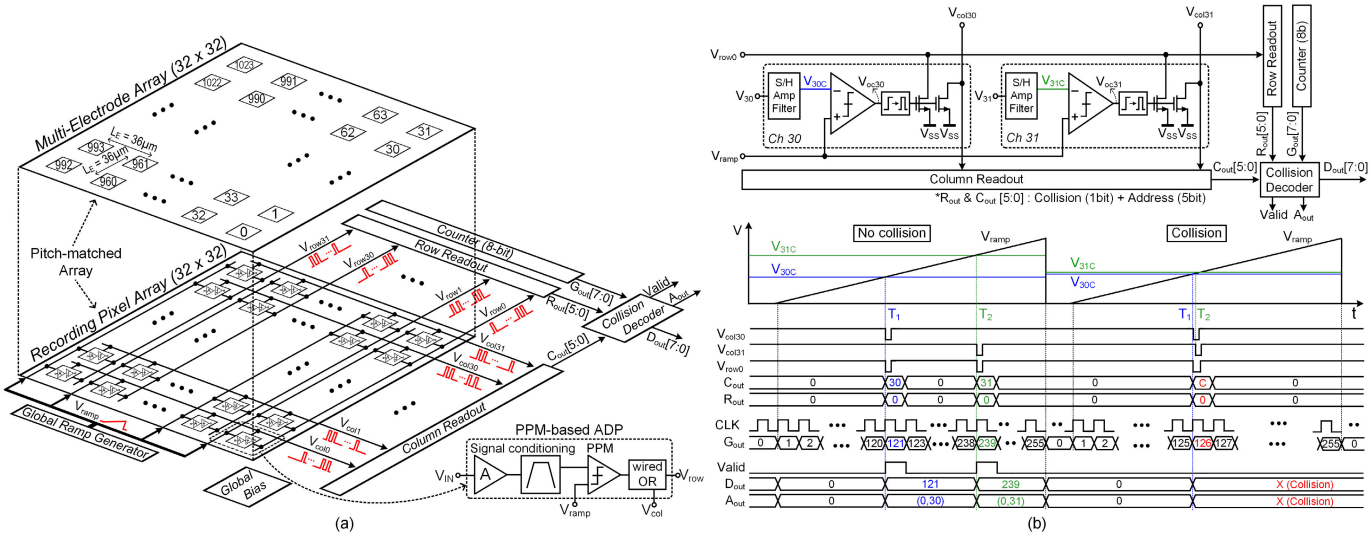


Fig. 3. (a) Chip architecture and (b) operation principle: two-channel example and its timing diagram.

$N \times N$ array is simultaneously read out with a reduced number of wires (from $N^2$ to $2N$ when compared with conventional analog and/or PPM-based pixels). Outside the array, the collision decoder reads the wired-OR PPM outputs and assigns the corresponding digital values based on a global counter synchronized with the ramp generator. If multiple pixels access the row/column buses during the same ramp step, decoding is not possible. These events are called collisions and are discarded (i.e., not stored) by the decoder performing data compression. Hence, only data from pixels having a unique digital value within a single ramp period are stored (see [20] and [21] for extensive validation of the wired-OR compression algorithm).

The described architecture has various advantages over the prior works. First, the PPM-based ADP includes only a single comparator for A/D conversion, which reduces its area and power consumption (the global ramp generator is shared among all pixels, making its power and area consumption negligible). Second, routing congestion in the array is significantly mitigated, allowing an increase in the number of channels while reducing the channel pitch (i.e., increasing the size and density of the array). Finally, since the compression occurs during A/D conversion and is realized without spike detection, the readout chain does not have massive data movement and spike detection overhead. Therefore, this analog-to-digital compression architecture enables simultaneous recording in large-scale MEAs while addressing the data deluge problem.

### B. Neural Recording IC Operation Principle

Fig. 3(a) shows the neural recording IC architecture. The recording pixel array has 1024 PPM-based ADPs, and its pixel pitch is matched to the electrode pitch ($L_E = 36$ $\mu$m) of the MEA to directly read out each electrode. The output of each ADP is read out by their row and column address location outside the array through the row and column wires ($V_{\text{row0}} - V_{\text{row31}}$ and $V_{\text{col0}} - V_{\text{col31}}$). Then, the row and column readouts process all row and column wires in parallel at each ramp step and output the collision information ($R_{\text{out}}[5]$ and $C_{\text{out}}[5]$) and addresses of the active pixels ($R_{\text{out}}[4{:}0]$ and $C_{\text{out}}[4{:}0]$). The collision decoder reads $R_{\text{out}}[5{:}0]$ and $C_{\text{out}}[5{:}0]$ at each of the 256 ramp steps and combines it with the output of an 8-bit counter ($G_{\text{out}}[7{:}0]$) to perform the 8-bit PPM. Finally, it outputs the address ($A_{\text{out}}$) and data ($D_{\text{out}}$) for the collision-free channels with a data valid flag (Valid).

Fig. 3(b) shows a two-channel example and its timing diagram. Each PPM-based ADP consists of a sample and hold ($f_s = 20$ kHz), an amplifier, filter, and a continuous-time (CT) comparator that drives the local row and column using

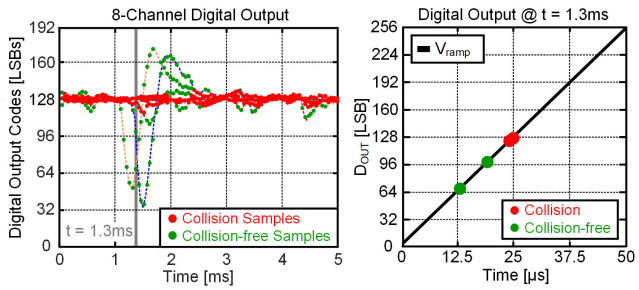


Fig. 4. Left: data compression example with primate retina recording (ex vivo). Right: example of pixel activity on the global ramp for a single sample at $t$ = 1.3 ms.

open-drain outputs. First, the acquired samples of each channel ($V_{30}$ and $V_{31}$) are amplified and filtered ($V_{30C}$ and $V_{31C}$) and then compared with $V_{ramp}$. The ramp crossing occurs at $T_1$ for channel 30, and it makes the comparator output ($V_{oc30}$) high, which triggers the corresponding wired-OR outputs ($V_{row0}$ and $V_{col30}$). In the same way, $V_{row0}$ and $V_{col31}$ are triggered at $T_2$ for channel 31. Then, the row and column readouts output the corresponding $R_{out}$[4:0] (=0 for both) and $C_{out}$[4:0] (=30 and 31) at $T_1$ and $T_2$ with the collision/no-collision information ($R_{out}$[5] and $C_{out}$[5]). The 8-bit PPM outputs at $T_1$ and $T_2$ are obtained from $G_{out}$[7:0] by the collision decoder along with the $R_{out}$[5:0] and $C_{out}$[5:0]. In the case that the two channels have different PPM outputs [Fig. 3(b) (bottom left)], the collision decoder outputs $A_{out}$ and $D_{out}$ of each channel with Valid = 1 (*no collision*). However, if the input values are so close that $T_1$ and $T_2$ occur in the same ramp step, the two channels have the same PPM outputs [Fig. 3(b) (bottom right)]. In this case, a collision occurs, and the outputs of the decoder ($A_{out}$ and $D_{out}$) are not valid (Valid = 0), thus discarded.

Fig. 4 shows an example of the data compression with eight-channel data recorded from ex vivo primate retina [23], [24]. A MATLAB behavioral model is used to emulate the array digitization, including the wired-OR compression. As can be seen, the wired-OR compression discards a large number of unwanted samples near the baseline of the neural signals where the probability of having the same PPM outputs is high. In contrast, it retains the more important spike samples of neural signals. This is because spike samples are rare, making the probability of collisions very low.

## III. Architectural Benefits

To investigate the benefits of the wired-OR architecture, the readout energy and output data rate of the entire array are compared with those of a conventional ADP array.

### A. Read-Out Energy Reduction

Fig. 5(a) shows the readout energy of a 1024-channel 8-bit ADP array. For simplicity, the required readout energy/bit for all pixels is assumed to be the bitline access cost $CV^2$ (assuming 1 V and 0.1 pF for 1-mm bitline). Then, the readout energy/pixel is 0.8 pJ for an 8-bit ADP, and the total energy to read out the entire array is 819.2 pJ (Fig. 6).

Fig. 5(b) shows the readout energy of a 1024-channel PPM-based ADP array. With the same assumption, since the PPM

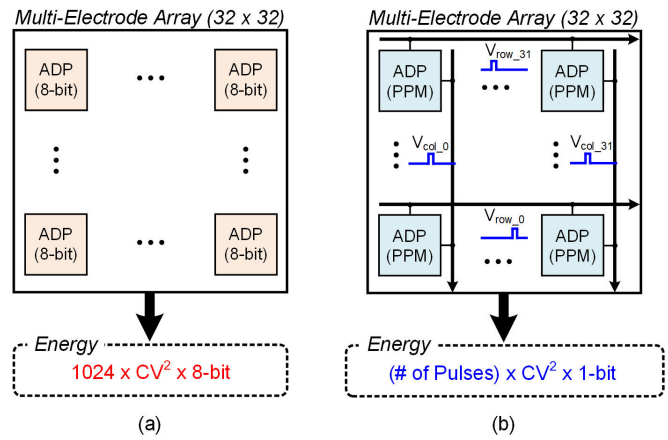


Fig. 5. Readout energy of (a) 1024-channel 8-bit ADP array and (b) 1024-channel 8-bit PPM-based ADP array.

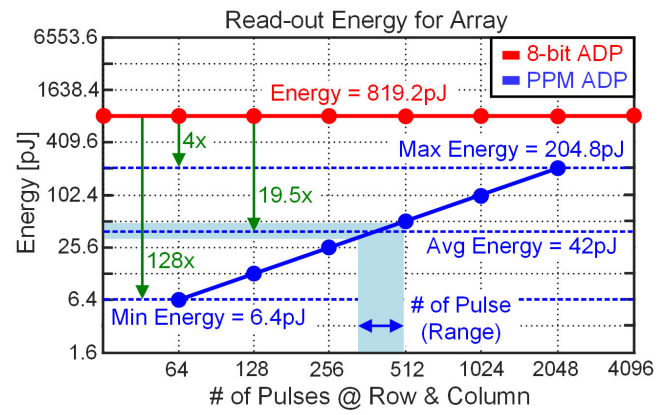


Fig. 6. Readout energy of 1024-channel 8-bit ADP array and 8-bit PPM-based ADP array according to the number of pulses.

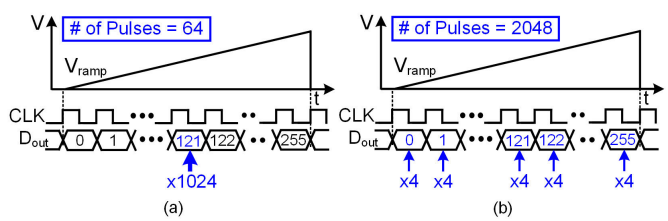


Fig. 7. Total number of pulses in 8-bit PPM-based ADP array during single ramp period. (a) Minimum case. (b) Maximum case.

ADP has a single-bit output on each wire (row and column), the required readout energy/wire is 0.1 pJ. Therefore, the readout energy for a 1024-channel PPM-based ADP array is equal to the total number of pulses on row and column wires during the entire ramp period multiplied by 0.1 pJ and is plotted in Fig. 6. The total number of pulses is minimum when all 1024 pixels have the same PPM output [Fig. 7(a)]. This results in 64 pulses in a single ramp step and a readout energy equal to 6.4 pJ. In contrast, the number of pulses is maximum when the PPM outputs of all pixels are evenly distributed with a unique row and column address. For example, four pixels having a unique row and column address are fired at each ramp step [Fig. 7(b)]. This results in eight pulses at each ramp step and a readout energy equal to 204.8 pJ. Therefore, the readout energy is input-dependent (ranging from 6.4 to 204.8 pJ) and is

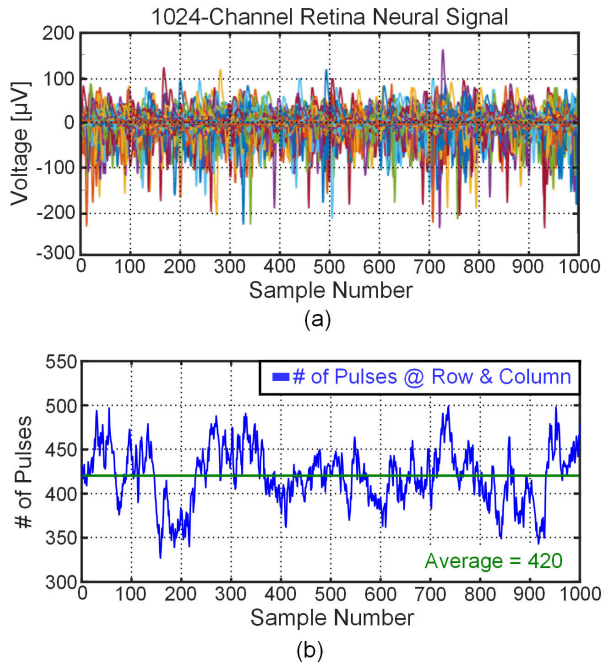


Fig. 8. (a) 1000 samples (=50-ms recording) of 1024-channel prerecorded retina neural signals. (b) Distribution of the total number of pulses at 1024-channel 8-bit PPM-based ADP array with the input signals of (a).

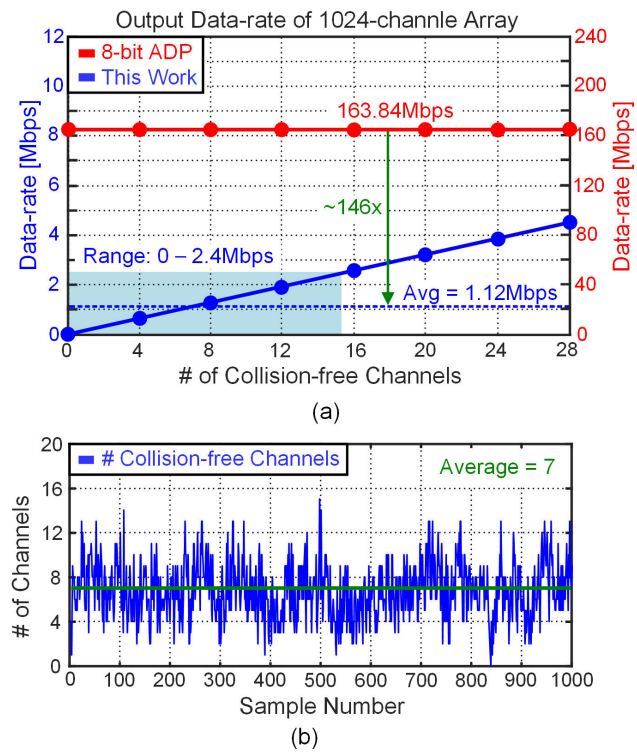


Fig. 9. (a) Data rate of 1024-channel 8-bit ADP array and 8-bit PPM-based ADP array with wired-OR compression. (b) Distribution of the number of collision-free channels with the input signals in Fig. 8(a).

4× to 128× lower than in the conventional case (Fig. 6). However, both extreme cases are unlikely, considering the statistics of the neural signal. Instead, the average readout energy should be estimated based on real neural signals. Fig. 8(a) shows 1000 samples for 1024 channels of pre-recorded neural signals from ex vivo primate retina [23], [24], which corresponds to 50-ms recording at 20-kHz sampling rate. These neural signals are used as input to the behavioral model described in Section II-B to obtain the total number of pulses per sample [Fig. 8(b)]. The total number of pulses ranges from 325 to 499 with the average number being 420, which corresponds to an average readout energy of 42 pJ. Therefore, the average readout energy reduction is 19.5× when compared with an 8-bit conventional ADP array.

### B. Output Data-Rate Reduction

With a typical sampling frequency of 20 kS/s, the output data rate of the 1024-channel 8-bit ADP array ($D_{\mathrm{ADP}}$) can be calculated as follows:

$$D_{\mathrm{ADP}} = 1024 \times 8 \text{ bit} \times 20 \text{ kS/s} = 163.84 \text{ Mb/s}. \quad (1)$$

In the case of a 1024-channel PPM-based ADP array with wired-OR compression, 8-bit output data are transmitted at 20 kS/s only when the channels are collision-free. Therefore, the output data rate ($D_{\mathrm{wOR}}$) depends on the total number of collision-free channels ($\mathrm{N_{cf}}$) and can be calculated as follows:

$$D_{\mathrm{wOR}} = \mathrm{N_{cf}} \times 8 \text{ bit} \times 20 \text{ kS/s}. \quad (2)$$

Fig. 9(a) shows the output data rate as a function of the number of collision-free channels. Since the number of collision-free channels is input-dependent, the output data rate also should be estimated based on the statistics of the neural signal as done for the readout energy. The number of collision-free channels ranges from 0 to 15, with an average number of 7 [Fig. 9(b)], corresponding to an average data rate of 1.12 Mb/s. Therefore, a data rate reduction of around 146× can be obtained compared with the 1024-channel 8-bit ADP array [Fig. 9(a)]. Even with this large compression rate, the reconstructed signal still retains the critical samples belonging to spikes and allows for efficient spike sorting, cell type classification, and recovery of cell map features [20], [21].

## IV. Implementation Details

### A. Overall Architecture

Fig. 10 shows the top schematic of the neural recording IC. In the neural recording front end, an ac-coupled low-noise boxcar (LNB) sampler and a low-pass filter (LPF) are implemented for sample and hold, amplification, and filtering, which are followed by a CT comparator to compare the input signal against the global ramp signal ($V_{\mathrm{RAMP}}$) and the wired-OR logic. The local clock generator provides all the phases for the recording front end from the system clock ($f_{\mathrm{ck}}$). The reference electrode is built-in on-chip and implemented with an electrode ring around the 32 × 32 MEA, which is actively driven by the neural recording IC.

The row and column pulse readout comprises a pulse detector for each row/column wire and a decoder. The pulse detector samples the output of the wired-OR logic using a negative-edge triggered flip-flop and uses a tunable pull-up current source to reset the wired-OR line ($I_{\mathrm{pull\text{-}up}}[3{:}0]$). The pulse decoder uses one-hot detection on the row/column wires to detect a collision ($R_{\mathrm{out}}[5]$ and $C_{\mathrm{out}}[5]$) and performs one

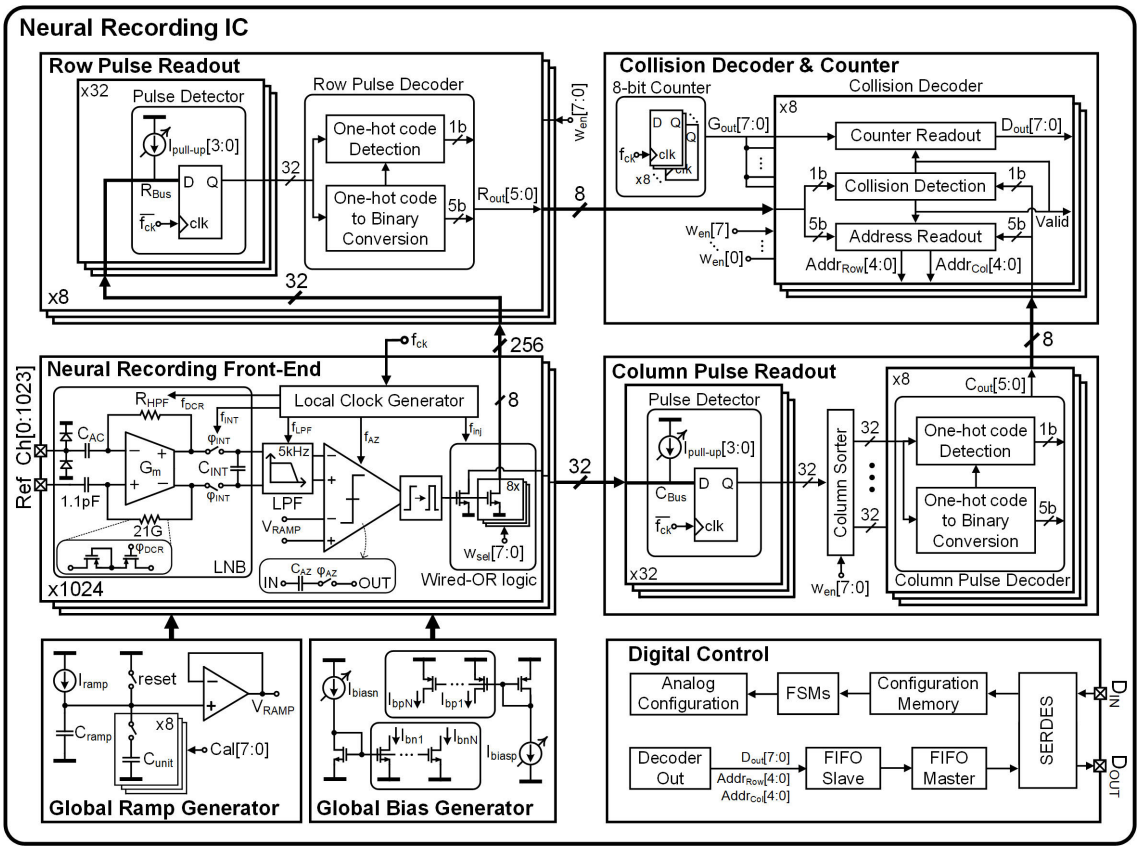


Fig. 10. Top schematic of the neural recording IC.

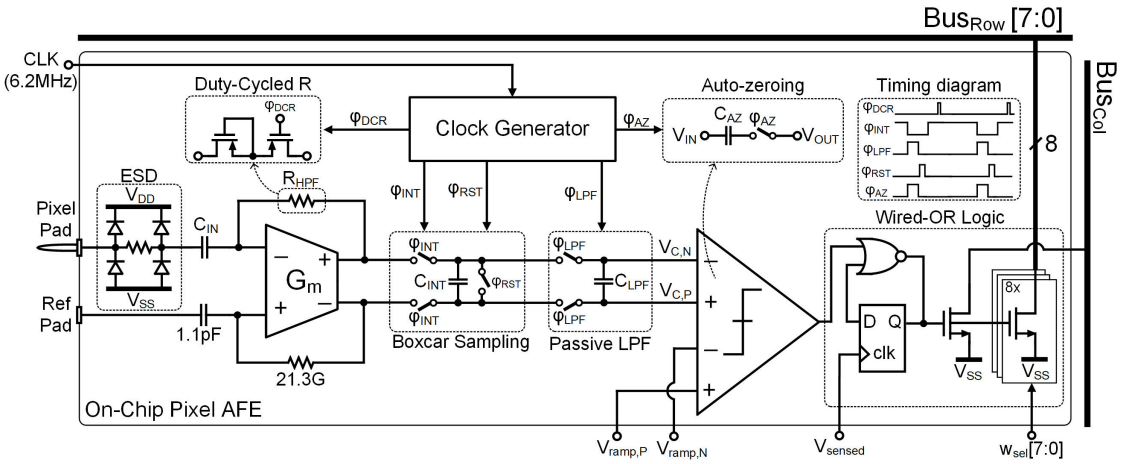


Fig. 11. Architecture of neural recording front end and its timing diagram.

hot to binary conversion to output the address of the active row/column wires ($R_{\text{out}}$[4:0] and $C_{\text{out}}$[4:0]).

The collision decoder outputs the row and column address together with the associated value from the global counter ($\text{Addr}_{\text{Row}}$[4:0], $\text{Addr}_{\text{Col}}$[4:0], and $D_{\text{out}}$[7:0]) and a flag signaling whether the output is collision-free or not (Valid). Using up to eight wires ($w_{\text{en}}$[7:0]) per row and column, the array can be split into multiple sub-arrays. This generates multiple levels for collision decoding and allows to control the collision rate (i.e., degree of compression).

The global ramp generator consists of a current source ($I_{\text{ramp}}$) and a tunable capacitor bank ($C_{\text{ramp}}$ and $C_{\text{unit}}$ with Cal[7:0]), followed by a unity-gain buffer to drive the 1024 channels. Also, a global bias generator provides the current bias ($I_{\text{biasp}}$ and $I_{\text{biasn}}$) to each pixel. The digital control unit is used to configure the chip and transmit the output data ($\text{Addr}_{\text{Row}}$[4:0], $\text{Addr}_{\text{Col}}$[4:0], and $D_{\text{out}}$[7:0]) off the chip using serial communication. The $f_{\text{ck}}$ is 6.2 MHz, and the input sampling rate ($f_s$) is 20 kS/s.

### B. Neural Recording Front End

Fig. 11 shows the architecture of the neural recording front end and its timing diagram. An ac-coupled LNB sampler minimizes the noise penalty from noise folding with its

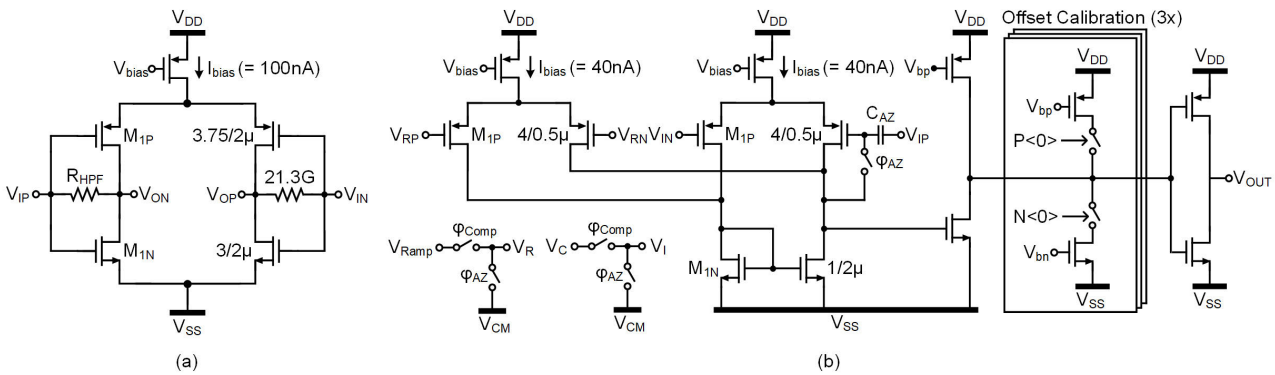


Fig. 12. Schematic of (a) front end $G_m$ and (b) continuous-time comparator with auto-zeroing and in-pixel output offset calibration.

inherent anti-aliasing property due to the notches at the multiples of sampling frequency (=20 kHz) and provides rail-to-rail electrode dc offset tolerance. To minimize area, the circuit uses a 1.1-pF input MOM capacitance ($C_{\mathrm{IN}}$) on top of ESD and active devices. The LNB uses an inverter-based $G_m$ with a large feedback resistor ($R_{\mathrm{HPF}} \cong 21.3$ G$\Omega$) for dc biasing and setting the high-pass corner ($f_{\mathrm{HP}} = 300$ Hz). The $R_{\mathrm{HPF}}$ is realized with a duty-cycled resistor (DCR), which consists of a 50-M$\Omega$ transistor in a triode region and a switch with 1/43 duty cycle ($\varphi_{\mathrm{DCR}} \approx 7.2T_{\mathrm{ck}}$), resulting in low noise and small area. The duty cycle is globally programmable with a 4-bit binary delay control unit. The output of the inverter-based $G_m$ is integrated on $C_{\mathrm{INT}}$ for $296T_{\mathrm{ck}}$ ($\varphi_{\mathrm{INT}}$) and then sampled on $C_{\mathrm{LPF}}$ for $8T_{\mathrm{ck}}$ ($\varphi_{\mathrm{LPF}}$) to implement a passive switched-capacitor low-pass filter (SC-LPF) without additional power consumption. The SC-LPF pole and the null from the boxcar result in an overall $f_{\mathrm{LP}} = 5$ kHz. The overall front end has a bandpass filter (BPF) response with a gain and bandwidth of 38 dB and 300 Hz–5 kHz; $6T_{\mathrm{ck}}$ are allocated to reset $C_{\mathrm{INT}}$ between samples ($\varphi_{\mathrm{RST}}$), which leads to $f_{\mathrm{ck}} = 310 f_s$ (=6.2 MHz). During the reset phase of the LNB, the outputs of the $G_m$ cell are connected to set the common-mode voltage, which is then copied to the input by the DCR resistor. During the integration phase, the previous sample stored in $C_{\mathrm{LPF}}$ is compared with the global ramp for PPM. The 8-bit conversion phase lasts $(256 + 40)T_{\mathrm{ck}}$ to compensate for the comparator latency. The comparator includes auto-zeroing ($\varphi_{\mathrm{AZ}}$) and in-pixel offset calibration to minimize the offset between channels to the level required by the wired-OR compression [20]. The ramp ($V_{\mathrm{ramp,P}}$ and $V_{\mathrm{ramp,N}}$) range and slope can be set to change the ADC resolution and input range of the pixel. In the wired-OR logic block, the comparator output trigger edge is converted into the pulse having a width of $T_{\mathrm{ck}}$ and synchronized to $f_{\mathrm{ck}}$ by the feedback synchronizer ($V_{\mathrm{sense}}$), resulting in an 8-bit PPM. Then, it is transmitted outside the array through the row and column OR buses. According to the array configuration for the number of wires ($w_{\mathrm{en}}$[7:0]), $w_{\mathrm{sel}}$[7:0] determines the channel connection to one of the row bus wires ($\mathrm{Bus}_{\mathrm{Row}}$[7:0]).

The $G_m$ cell is implemented with a current starved inverter self-biased by a DCR [Fig. 12(a)]. With a bias current of only 100 nA, the resulting $G_m$ is 2.8 $\mu$S, which corresponds to an integrated input-referred thermal noise of 6 $\mu$V$_{\mathrm{rms}}$ over 1 Hz–10 kHz. The input-referred noise contribution from the

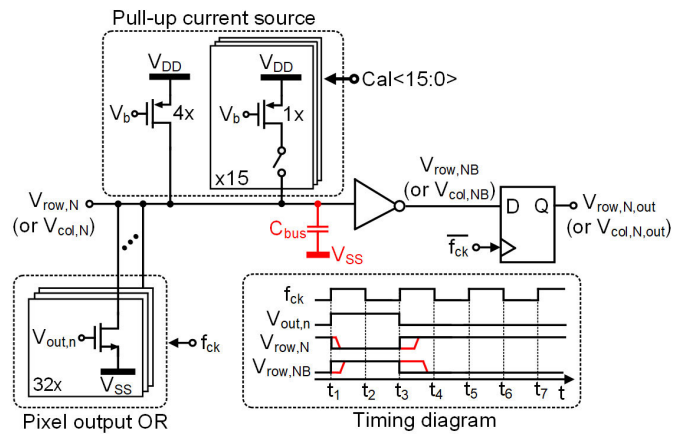


Fig. 13. Schematic of row (or column) pulse read-out circuit and its timing diagram.

DCR is designed to be negligible (= 2.3 $\mu$V$_{\mathrm{rms}}$) compared with $G_m$, while it only occupies an area of 1.6 × 2.8 $\mu$m$^2$. Even with the $G_m$ cell device size of 13.5 $\mu$m$^2$, the standard deviation of the recording front-end's input-referred offset is 18 $\mu$V$_{\mathrm{rms}}$ based on Monte Carlo simulations because of the auto-zeroing at the comparator. The CT comparator is implemented with four inputs differential to single-ended architecture [Fig. 12(b)]. It consumes 80 nA in the input pairs (40 nA per branch), which are sized, such that, when combined with auto-zeroing, the offset of the comparator does not degrade the noise and offset performance of the pixel. In-pixel offset calibration circuits are added at the single-ended output to further reduce the offset variation across pixels. By adjusting the amount of sink and source offset current at the output, a delay in the CT comparator output is introduced, which is equivalent to controlling the ADC digital output value. The maximum calibration range is ±7 LSB, which corresponds to 17.9-$\mu$V input-referred offset.

### C. Row and Column Pulse Readout

Fig. 13 shows the schematic of the row (or column) pulse readout circuit and its timing diagram. The 4-bit programmable pull-up current source drives 32× pixel output OR logic and its bus routing line ($V_{\mathrm{row,N}}$ or $V_{\mathrm{col,N}}$). As soon as one of the comparator output pulses ($V_{\mathrm{out,n}}$) at a row (or column) triggers the output OR logic, the $V_{\mathrm{row,N}}$ (or $V_{\mathrm{col,N}}$) goes low, and the

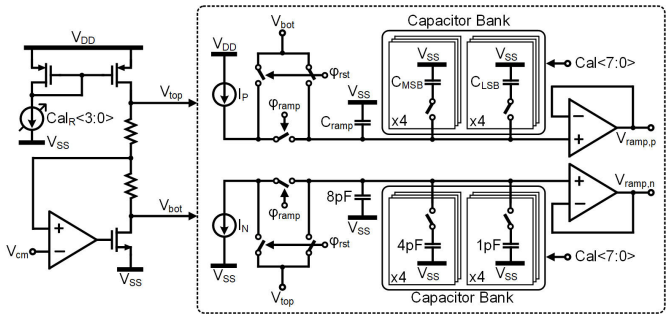


Fig. 14. Schematic of the global ramp generation circuit.

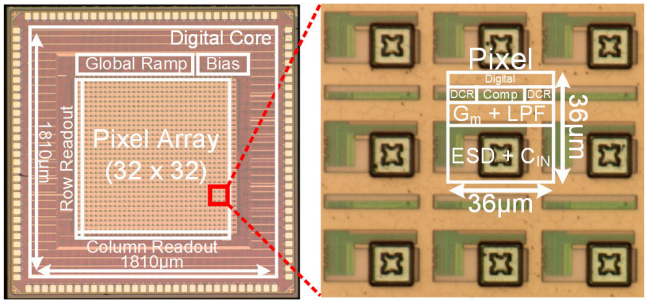


Fig. 15. Die photograph.

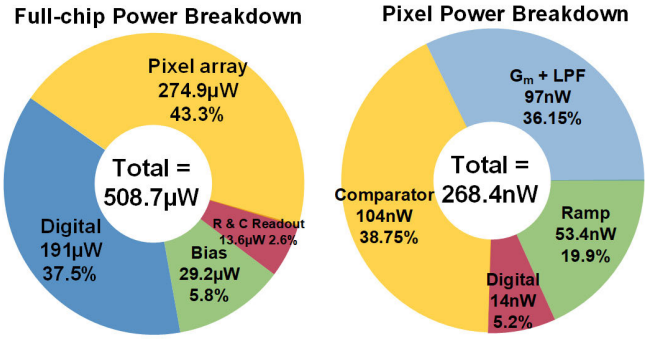


Fig. 16. Power breakdown of full chip and pixel.

buffered output $V_{\text{row,NB}}$ (or $V_{\text{col,NB}}$) goes high. Then, the $V_{\text{row,NB}}$ (or $V_{\text{col,NB}}$) is sampled by the flip-flop at the opposite phase of $f_{\text{ck}}$ ($t_2$), and the pulse output $V_{\text{row,N,out}}$ (or $V_{\text{col,N,out}}$) of the $N$th row (or column) is transmitted to the row (or column) pulse decoder. If the parasitic capacitance ($C_{\text{bus}}$) from the 32× pixel output OR logic and the $V_{\text{row,N}}$ (or $V_{\text{col,N}}$) bus routing is so large, such that the pull-up current source cannot charge it within a half $f_{\text{ck}}$ cycle, multiple counts of the pulse occur (e.g., double count occurs if $V_{\text{row,NB}}$ is still high even after $t_4$). Therefore, the pull-up current source is designed to have its row (or column) driving capability.

### D. Global Ramp Generator

Fig. 14 shows the schematic of the global ramp generation circuit. The ramp starting points ($V_{\text{top}}$ and $V_{\text{bot}}$) are generated by a regulated resistor divider around the common mode voltage ($V_{\text{cm}}$) and are programmable with 4-bit resolution ($\text{Cal}_{\text{R}}$[3:0]). The source and sink current sources ($I_{\text{P}}$ and $I_{\text{N}} =$ 15 nA) and the capacitors, including $C_{\text{ramp}}$ and the tunable capacitor bank ($C_{\text{MSB}}$ and $C_{\text{LSB}}$), determine a ramp slope, which is adjustable with 8-bit resolution. The resulting input range of the pixel is from 0.75 to 2.25 $\text{mV}_{\text{pp}}$. The reset and ramp timing ($\varphi_{\text{rst}}$ and $\varphi_{\text{ramp}}$) is equal to the reset and integration timing of the pixel. Finally, the unity gain buffer is designed to have the driving capability of a 1024-channel array, including gate and routing parasitic to ensure even distribution of the ramp signals ($V_{\text{ramp}},p$ and $V_{\text{ramp}},n$) across the array.

## V. Measurement Results

### A. Electrical and In Vitro Measurements

The prototype IC was fabricated in a 28-nm standard CMOS process with a 1-V supply voltage. It occupies a total active area of 3.27 $\text{mm}^2$. The size of the 1024-channel array is 1.2 × 1.2 $\text{mm}^2$, and the size of each pixel is only 36 × 36 $\mu\text{m}^2$ (≃0.00129 $\text{mm}^2$) with a 15 × 15 $\mu\text{m}^2$ electrode deposited directly on top. As shown in Fig. 15, the pixel area is dominated by the ESD protection diode and the input capacitor.

Fig. 16 shows a power breakdown of the full chip and the pixel. The measured total power consumption of the neural recording IC is 508.7 $\mu$W, and the corresponding chip total power per channel is 496 nW. It should be noted that the power consumption of the pixel array and digital part dominate, while the row and column readouts are only 2.6% of the total. The total power consumption of the pixel is only 268.4 nW, and it is mostly dominated by the comparator and the $G_m$ cell. The power in the $G_m$ cell is limited by noise requirements, while the power in the comparator is limited by bandwidth requirements. Note that the pixel power also includes the power consumption from the ramp generation, which is shared among all channels and accounts for around 20% of the total pixel power budget. The digital power could be further reduced by supply voltage scaling and by introducing a multi-clock domain and implementing more aggressive clock gating, since the activity in the processing pipeline is mostly driven by collision-free events.

Fig. 17(a) shows the measured pixel frequency response. The bandpass filter response is obtained with a high-pass and low-pass pole of 300 Hz and 5 kHz, respectively, and an in-band gain of 38 dB, which is well matched with the simulation results. Fig. 17(b) shows the measured output spectrum of the single pixel when a 1-kHz, 1-$\text{mV}_{\text{pp}}$ sine wave is applied at the input. Under these conditions, the pixel achieves a peak SNDR and SFDR of 34 and 63 dB, respectively, and the corresponding input-referred noise is 7 $\mu\text{V}_{\text{rms}}$.

Fig. 18 shows the in vitro test setup and neural spike recording result with a single channel. The platinum (Pt) electrodes of 15 × 15 $\mu\text{m}^2$ were deposited on each pixel post-fabrication, and the pre-recorded retina neural signals were injected in saline solution using an arbitrary waveform generator (Keysight 33500B) connected to a platinum wire. The neural recording IC was encapsulated after wire bonding, so that only the MEA was exposed to saline solution. The measured retina neural spike waveform shows that even with small and high-impedance (≈1.15 MΩ at 1 kHz) electrodes, the IC can accurately record neural spikes.

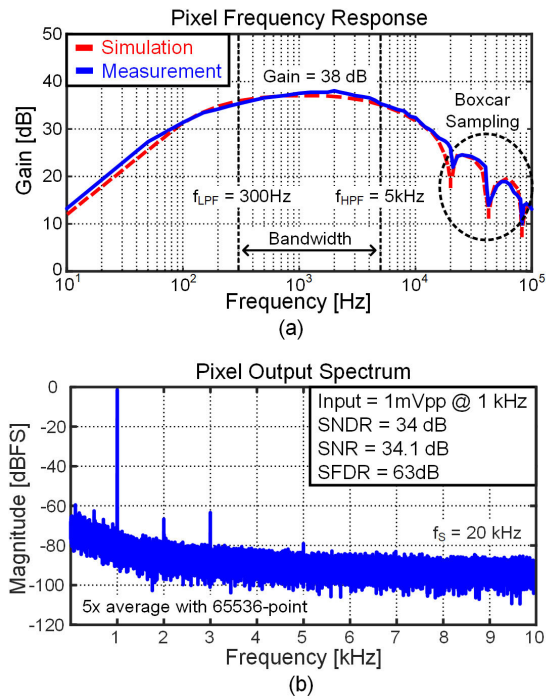


Fig. 17. Measured single-channel characteristics. (a) Frequency response. (b) Output spectrum.

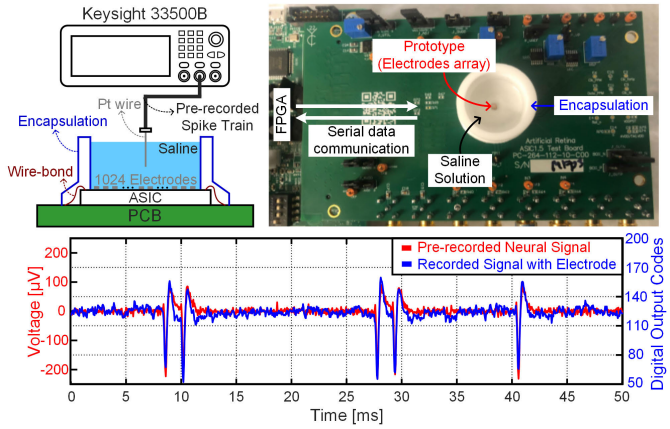


Fig. 18. In vitro test setup and measured neural spike waveform.

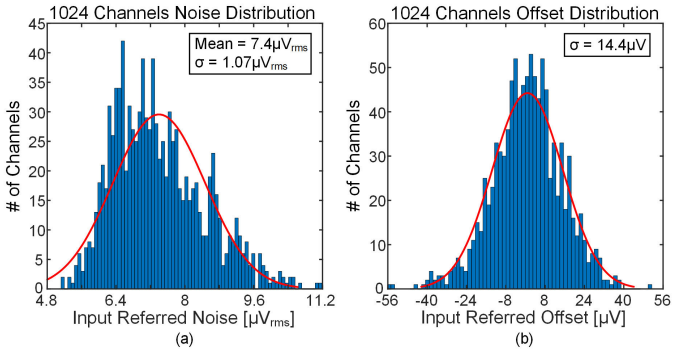


Fig. 19. Measured 1024-channel characteristics. (a) Noise distribution. (b) Offset distribution.

Fig. 19 shows the measured input-referred noise and offset distribution of all 1024 channels. The saline solution is grounded in the in vitro test setup (Fig. 18), and sputtered iridium oxide film (SIROF) electrodes are additionally deposited on each pixel to reduce the electrode impedance (≈250 kΩ at 1 kHz). The mean and standard deviation of the 1024-channel array are 7.4 and 1.07 $\mu V_{rms}$[1] [Fig. 19(a)], respectively, which shows an even pixel noise characteristic over the entire array. The measured 1024-channel input-referred offset distribution is shown in Fig. 19(b). The standard deviation of input-referred offset for the 1024-channel array is 14.4 $\mu$V, which is within the pixel-to-pixel offset calibration range of 18 $\mu$V.

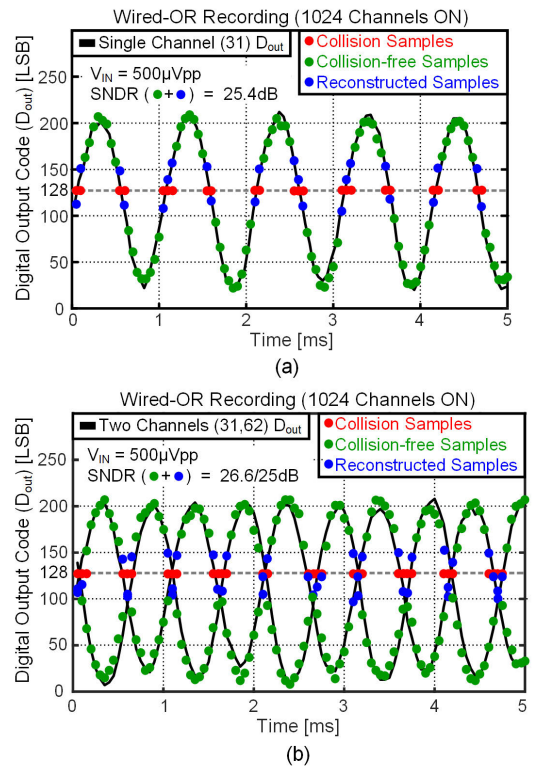


Fig. 20. Measured sinewaves with wired-OR compression. (a) Single channel recording. (b) Two channels recording.

Fig. 20 shows sine-wave measurements to visualize the wired-OR compression. A sine wave is applied to a single channel, while all other channels are connected to the grounded saline solution [Fig. 20(a)]. As can be seen, all samples outside the baseline are captured, while missing samples near the baseline are reconstructed using an interpolation filter. The interpolation is performed with a three-tap non-causal finite impulse response (FIR) filter with coefficients $b_{-1} = 0.5, b_0 = 0$, and $b_{+1} = 0.5$. Fig. 20(b) shows data-compressive sine-wave measurement with two active channels. All critical samples for reconstructing the two signals are still captured, since the two sinewaves are out of phase and rarely present the same digital value at the same time.

Fig. 21 shows data-compressive measurements of a retinal neural spike signal. The pre-recorded neural signal is applied to a test channel, while all other channels are connected to the grounded saline solution. As can be seen, all the spike samples

[1] In [22], the numbers were measured with Pt electrodes deposition on each pixel. Those are revised to the measured values with the additional deposition of SIROF electrodes on each pixel.

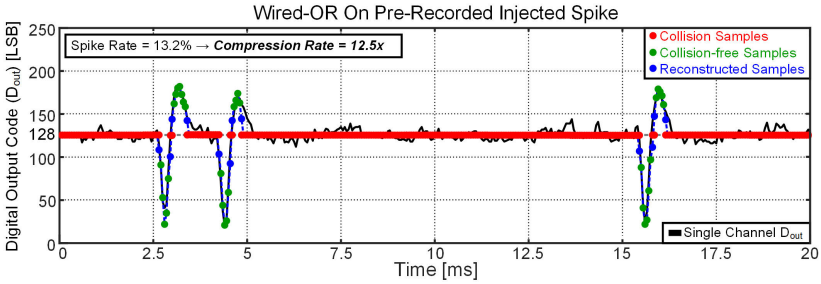


Fig. 21. Measured pre-recorded injected neural spikes with wired-OR compression.

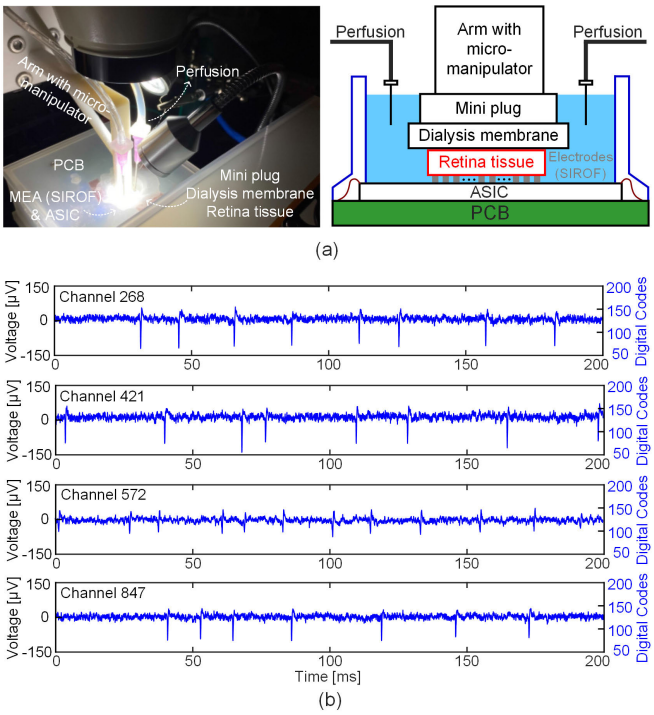


Fig. 22. (a) Ex vivo test setup. (b) Measured neural signals.

are well captured, while the baseline samples are discarded. The missing samples near the baseline are also reconstructed using a simple interpolation filter. The compression rate is inversely proportional to the spike rate. Here, a 12.5× compression rate is achieved with an artificially large spike rate of 13.2% (10× larger than typical spike rates).

### B. Ex Vivo Validation

The neural recording IC was further validated through an ex vivo experiment with a rat retina. Fig. 22(a) shows the experimental setup used to obtain ex vivo recordings. Dissected rat retina tissue is flattened onto the MEA using a mini-plug covered with a dialysis membrane controlled by a micro-manipulator, so that the retinal ganglion cells are close to the SIROF electrodes. The ex vivo tissue is perfused with perfluoro liquid to keep it healthy during the experiment.

The recording IC is able to recover spikes with high fidelity during single-channel recordings without compression—see Fig. 22(b). Spikes can also be recovered when the wired-OR algorithm is enabled, and all 1024 channels are active—see Fig. 23. As expected, the number of wires configured in

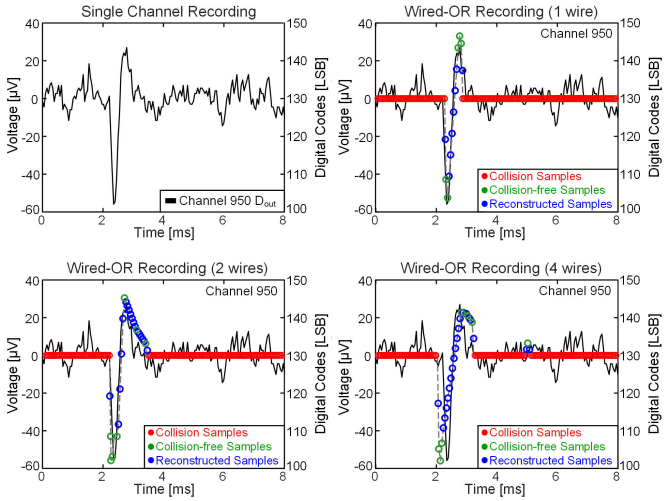


Fig. 23. Measured neural spikes with wired-OR compression according to the number of wires (ex vivo). Reconstructed spikes during wired-OR recordings are compared against average spikes during single-channel recordings.

the array controls the compression-accuracy trade-off. In this experiment, the average spike rate is 30.6 spikes/s, and the compression rate ranges from 111.2× to 38.8× with one wire and four wires, respectively. Here, compression is defined as the number of collision-free channels over the total 1024 channels for every sample. Waveform distortion can compromise certain BCI tasks where spike sorting is needed. The analysis of this compression-accuracy trade-off is beyond the scope of this article. The reader can refer to our previous work in [20] and [21] for an extensive analysis of this trade-off across multiple experimental datasets.

### C. Comparison With State-of-the-Art Works

Table I shows the performance summary and comparison with other state-of-the-art neural recording ICs [9], [10], [17], [25], [26], [27], [28], [29]. This work focuses solely on action potentials, which have been shown to achieve the highest performance in motor BCI tasks when compared with local field potentials [5]. As a result, the AFE bandwidth is limited to high-frequency content, and the required ADC resolution is limited to 8 bits [5]. With the largest number of channels, this work achieves the lowest power consumption per channel with sufficiently low input-referred noise (IRN) required for effective neural recording. Especially, *power/Ch* and *chip total power/Ch* are significantly reduced to hundreds of nW levels, which are 10.1× and 16.8× lower than the best prior works,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WORKS

| | **This work** | [25] | [17] | [10] | [26] | [27] | [9] | [28] | [29] |
|---|---|---|---|---|---|---|---|---|---|
| Technology [nm] | **28** | 22 | 180 | 65 | 55 | 130 | 180 | 180 | 130 |
| Supply [V] | **1.0** | 0.8 | 1.8 | 1.2 | 1.2 | 1.2 | 0.5/1/1.8 | 0.5 | 1.2 |
| Input type | **AC-coupled** | AC-coupled | DC-coupled | AC-coupled | DC-coupled | AC-coupled | AC-coupled | AC-coupled | AC-coupled |
| Topology | **Boxcar + SS ADC** | 1st order ΔΔΣ | 2 step IΔΣ | IA + SAR | 2nd order ΔΔΣ | IA + SAR | IA + ΔΔΣ | LNA + SAR | LNA + SAR |
| Type of signal | **AP** | LFP+AP | LFP+AP | LFP+AP | LFP+AP | LFP+AP | LFP+AP | AP | AP |
| # of Channels | **1024** | 128 | 8-24 | 1024 | 16 | 384 | 1024 | 16 | 64 |
| BW [Hz] | **300-5k** | 0.5-10k | 0.5-10k | 0.5-10k | 0.5-10k | 0.5-10k | 0.4-9.2k | 1-6.8k | 192-7.4k |
| ADC [bit] | **8** | - | 11 | 10 | - | 14 | 11/8 | 8 | 8 |
| Power/Ch [$\mu$W] | **0.268** | 6.02 | 8.59 | 2.72 | - | 48.7 | - | 0.88 | 3.04/4.54 |
| Chip Total Power/Ch [$\mu$W] | **0.496** | 8.34 | 14.94 | 24.08 | 61.2 | 95.1 | 15.35 | - | 5.15 |
| IRN [$\mu V_{rms}$] | **7.4 (AP)** | 7.71 (AP) 11.9 (LFP) | 4.37 (AP) 2.72 (LFP) | 8.89 (AP) 6.8 (LFP) | 5.53 (AP) 2.88 (LFP) | 7.43 (AP) 7.78 (LFP) | 5.18 (LFP+AP) | 5.4 (AP) | 3.8 (AP) |
| *NEF / PEF (AP band) | **2.84 / 8.07** | 9.6 / 73.7 | 4.85 / 42.4 | 15.3 / 282.8 | 15.2 / 278.2 | 25.5 / 650.3 | - / 59.4 | - | 3.32 / 13.27 |
| Input range [$mV_{pp}$] | **0.75-2.25** | 43 | 14 | 0.75-4.87 | 148 | 12.5 | - | - | - |
| THD [%] | **0.097 @-3dBFS** | 0.015 @21.5$mV_{pp}$ | 0.078 @10$mV_{pp}$ | 0.57 @-0.8dBFS | 0.05 @20$mV_{pp}$ | 0.17 @10$mV_{pp}$ | 0.062 @3.2$mV_{pp}$ | 2.2 @92$mV_{pp}$ | 0.08 @3$mV_{pp}$ |
| Area/Ch [$mm^2$] | **0.00129** | 0.0045 | 0.0046 | 0.0062 | 0.0077 | 0.035 | 0.098 | 0.16 | 0.16 |
| EDO Tolerance | **Rail-to-Rail** | Rail-to-Rail | ± 60 mV | Rail-to-Rail | ± 70 mV | Rail-to-Rail | Rail-to-Rail | Rail-to-Rail | Rail-to-Rail |

*NEF / PEF are calculated using Chip Total Power/Ch

respectively [10], [25]. This enables a sub-mW chip total power consumption even with a 1024-channel array. As a result, this work achieves the highest power efficiency among neural recording ICs with the best NEF and PEF of 2.84 and 8.07, respectively, advancing the PEF of the best state of the art by 5.2×. It should be noted that NEF and PEF are calculated by using *chip total power/Ch* to compare the power efficiency of the entire neural recording IC, which includes a signal acquisition chain (front-end amplifier and ADC, or only ADC in the cases of direct conversion), and digital back end. It also achieves the smallest area per channel (=0.00129 $mm^2$) among all neural recording ICs, advancing area efficiency of the best state of the art by 3.5×. This enables a single-cell resolution neural interface, while the wired-OR compression method significantly reduces the data deluge problem from massive MEA and immense data movement in the recording chain without any spike detection overhead.

## VI. CONCLUSION

A 1024-channel data-compressive neural recording IC is realized for future single-cell resolution high-bandwidth BCIs. It achieves a high-density and large-scale recording array by implementing PPM-based ADP, which significantly reduces routing congestion. By using a wired-OR data compression method, the data-deluge problem in large-scale MEAs is mitigated. Also, on-chip massive data movement and spike detection overhead are avoided, thus enabling massively parallel recording arrays. The prototype achieves the power consumption per channel of 268 nW and an area per channel of 36 × 36 $\mu m^2$ with 7.4-$\mu V_{rms}$ input-referred noise and 0.3–5-kHz bandwidth, which results in the best power and area efficiency among the neural recording ICs published to date. The neural recording IC architecture offers great promise in enabling massively parallel single-cell resolution MEAs for future BCIs.

## ACKNOWLEDGMENT

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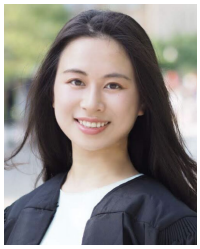

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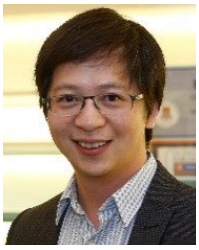

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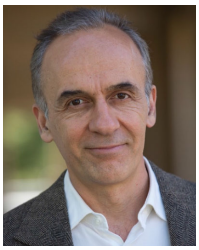

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